■ Description

IPS040 is the IC for simple Frequency Temperature Compensation combined with F0 adjustment, corresponding to the fundamental crystal from 20MHZ to 160MHz. F0 adjustment can independently be applied to 20MHz to 160MHz by turning off the temperature compensation function.

The temperature compensation using IPS040 is quite simple compare to common TCXO IC, so it is very easy to achieve High Precision SPXO.

■ Features

- Frequency Temp. deviation : ±10ppm Typ. ±5ppm achievable
- Operation temperature : -40 to 90℃
- Frequency dev. at room temp. : Within±1ppm
- F0 compensation range : Over ±30ppm
- Frequency stability to Vdd : Within ±1ppm
- Crystal frequency : 160MHz maximum
- Memory : Interchip original Non-volatile memory
- Pad number : 6 pads. No additional pin is necessary to program it
- Power supply voltage : 1.62～3.63V
- Standby function : Oscillation stop
- Output : CMOS
- Divide function : Divide is selectable by program
- Chip size : 0.74mm × 0.85mm
- Duty cycle : Within 50±5%

1. Part number rule

IPS : Series Name for SPXO
040 : Product Series
x : Frequency Range
M : VDD M : 1.62 ～3.63V
z : Oscillation Mode & Divide
A : Compensation
X : Pad Layout X : Cross F : Flip Chip
-W : IC Form
1 : Thickness

Mode	x	Frequency Range
Fundamental	5	20～160MHz

Frequency range by programming

40MHz Mode	20～60MHz
80MHz Mode	60～90MHz
120MHz Mode	90～130MHz
160MHz Mode	130～160MHz

Compensation	
A	F0 only
Blank	F0 + TC

z	Mode	Divide
0	Fundamental	1/1
R	Fundamental	1/1, 1/2, 1/4, 1/8 by program

IC Form	Thickness	Definition
-W	1	Wafer 150um
Blank or -C	Blank	Chip 150um

2. Series

Part Number	Output Frequency (MHz) Min.	Output Frequency (MHz) Max.	Divide	Compensation	Pad Layout	Remark
IPS040 5 M 0 A X	20	160	1/1	F0 only	Cross	
IPS040 5 M 0 X	20	160	1/1	F0 + TC		
IPS040 5 M 0 F	20	160	1/1		Flip Chip	
IPS040 5 M R A X	Crystal Frequency : 20MHz to 160MHz 1/1, 1/2, 1/4 and 1/8 is selectable by program. Default is 1/1.			F0 only	Cross	
IPS040 5 M R X				F0 + TC		
IPS040 5 M R F					Flip Chip	

3. Absolute Maximum Ratings Unless otherwise stated, V_{SS}=0V, Ta=25℃±2℃

Parameter	Symbol	Condition	Ratings Min	Ratings Max	Ratings Unit
Supply Voltage	V_{DD}	Program Mode	V_{SS}-0.5	7.0	V
		Oscillation Mode	V_{SS}-0.5	5.0	
Input Voltage	V_{IN}	All Input Pin	V_{SS}-0.5	V_{DD}+0.5	V
Output Voltage	V_{OUT}		V_{SS}-0.5	V_{DD}+0.5	V
Input Current	I_{IN}	CE Pin		50	μA
Output Current	I_{OUT}			25	mA
Junction Temperature	Tj		-55	150	℃
Storage Temperature	T_{stg}		-55	125	℃

4. Recommended Operating Condition

Unless otherwise stated, V_{SS}=0V, T a =- 40℃～+90℃

Parameter	Symbol	Condition	Min	Typ	Max	Unit	Note
Supply Voltage (Programming)	V_{DD}	Lo Vdd mode	1.62	3.30	3.63	V	V_{DD}
		Hi Vdd mode	2.25	3.30	3.63		
“H” Input Voltage	V_{IH}		V_{DD}×0.7			V	CE
“L” Input Voltage	V_{IL}				V_{DD}×0.3	V	CE
Input Voltage	V_{IN}		V_{SS}		V_{DD}	V	CE
Output Load Capacitance	CL	CMOS			15	pF	OUT
Ambient Temperature	T_{opt}		-40		90	℃	

This IC has enough immunity against ESD and Latch-up, but handle with care.

5. Electrical Specification

Parameter	Symbol	Condition	Specification			Unit
			Min	Typ	Max	
Out put Leak current	Iz	CE≦0.3V			10	μA
"L" input current	I_{IL}	CE pad, $V_{IN}=V_{SS}$		-10		μA
Oscillation Disable Time	Tplz	OUT pad			0.2	μs
Oscillation Enable Time	Tpzl	OUT pad			2	ms
Oscillation start up time	Tstart				2	ms
"H" output voltage	V_{OH}	OUT pad, I_{OH}=-4mA	V_{DD}-0.4			V
"L" output voltage	V_{OL}	OUT pad, I_{OL}=4mA			0.4	V
Current consumption	I_{DD}	CL=15pF, VDD=3.3V, CE≧VDD-0.3V, Low Voltage Mode				
		F0=40MHz		3.5	5.5	mA
		F0=80MHz		7.0	11.0	
		F0=120MHz		10.0	16.0	
		F0=160MHz		15.5	25.0	
		CL=15pF, VDD=3.3V, CE≧VDD-0.3V, High Voltage Mode				
		F0=160MHz		18.0	28.5	mA
Current consumption at oscillation disable	I_{DDD}	CL=15pF, VDD=3.3V, CE≦0.3V		1.5	5.0	μA
Frequency deviation at room temperature	F_0				±1	ppm
F_0 compensation range	F_{0r}		±30			ppm
Frequency Temperature deviation(Reference value)	Ftst	-40~90℃ Except IPS0405M0A		±5	±10	ppm
Frequency V_{DD} deviation	Fvst	V_{DD}±10%			±1	ppm
Output Duty Ratio	Duty	CL=15pF, VDD=2.25～3.63V	45	50	55	%
		CL=15pF, VDD=1.62～2.25V	43	50	57	
Rise/Fall time	Tr/Tf	CL=15pF, 10～90%VDD, VDD=1.62～3.63V				ns
		40MHz		2.5	6.0	
		80MHz		1.2	3.0	
		120MHz		1.2	3.0	
		160MHz		1.0	2.5	

Phase Noise of IPS040xMz
Frequency =40MHz, VDD = 3.3V

Offset	Phase Noise (dBc)
10Hz	-70
100Hz	-100
1KHZ	-128
10KHz	-148
100KHz	-156
1MHz	-160

Phase Noise of IPS0405M0A
Frequency =40MHz, VDD = 3.3V

Offset	Phase Noise (dBc)
10Hz	-85
100Hz	-113
1KHZ	-140
10KHz	-153
100KHz	-158
1MHz	-160

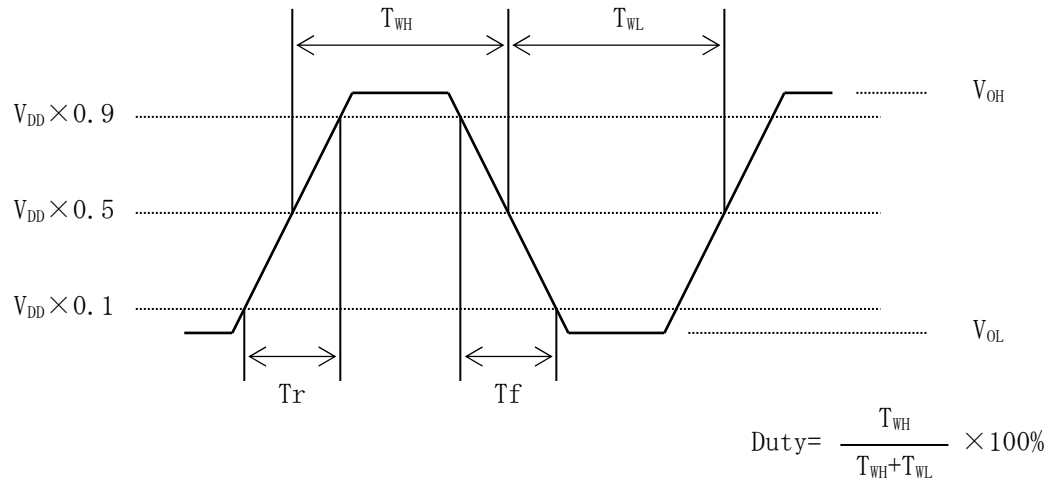
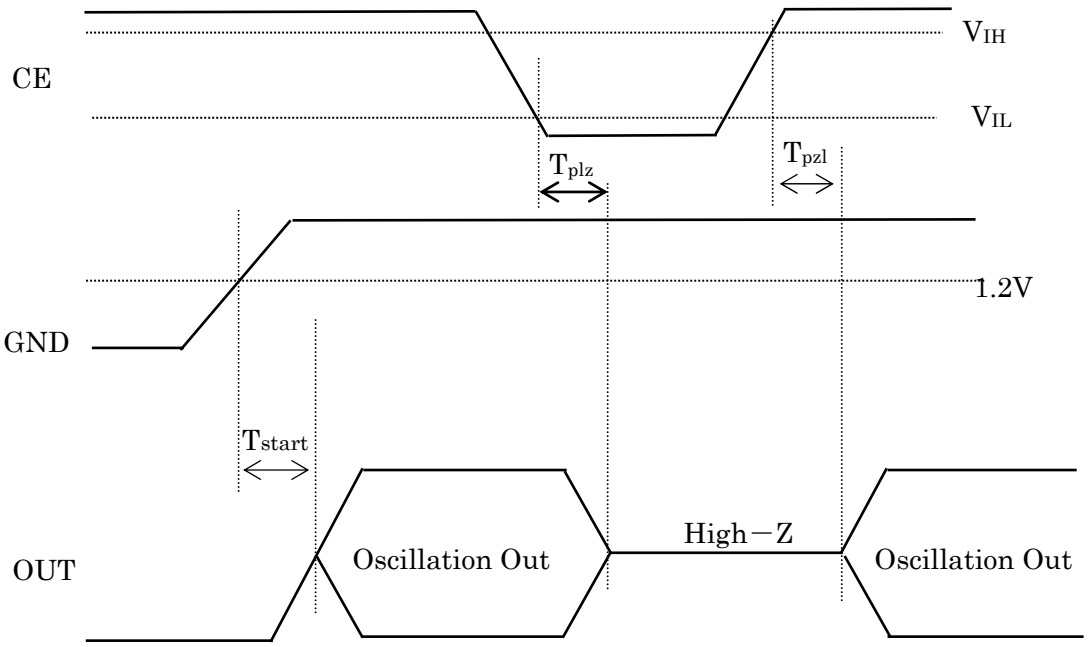


Fig. 5-1 Output wave form (Duty, Tr, Tf, V_{OH}, V_{OL})



V_{IH} : Threshold voltage for Oscillation Start
V_{IL} : Threshold voltage for Oscillation Stop

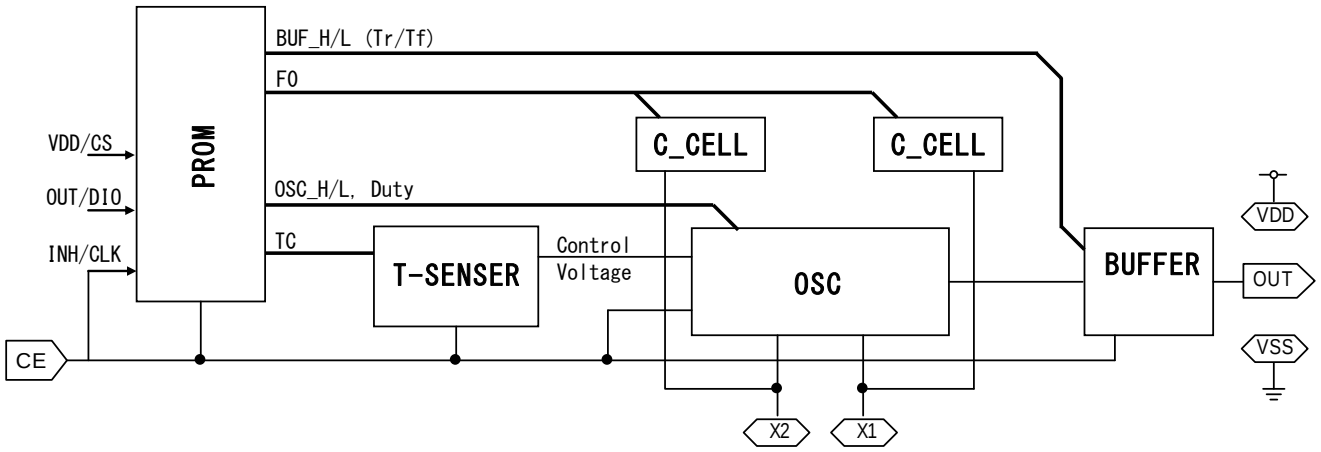
Fig. 5-2 Input output signal timing

6. Circuit Parameters of Oscillator (Reference Data for Circuit Design)

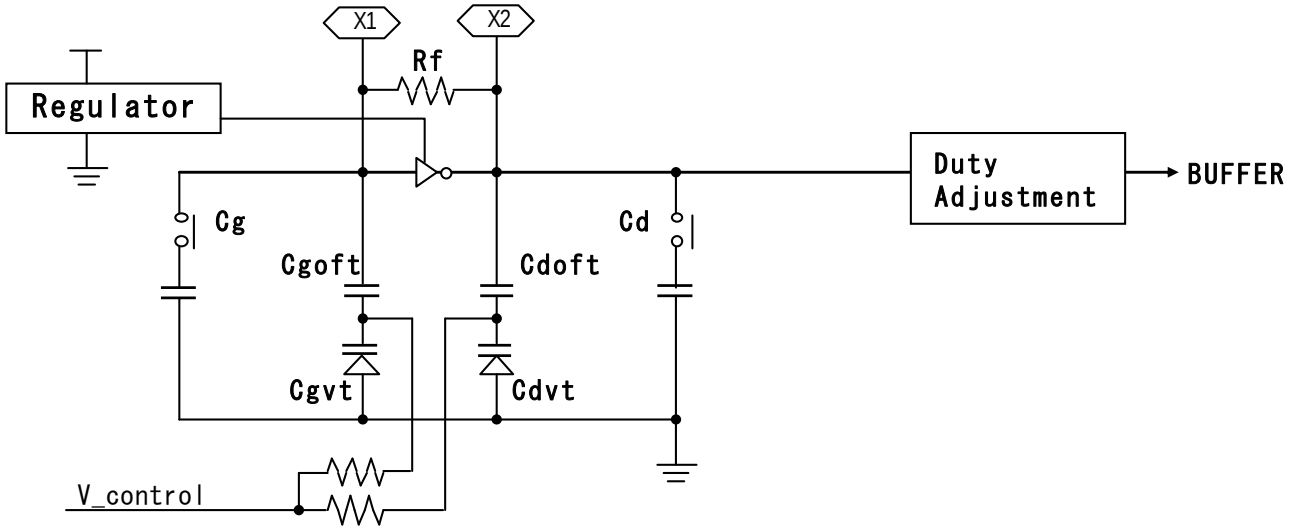
Ta=25℃, V_{DD}=3.3V

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Equivalent series (Loading) Capacitance	CLxtal	IPS040xMz, V_{DD}=3.3V, f_{xtal}=40MHz		4.0		pF
Drive Level	DL	V_{DD}=3.3V, Ta=25℃ f_{xtal}=40MHz		50		μW
Regulated Voltage	Vreg	Low Voltage Mode [A01]=[0]		1.5		V
	R_{V2}	High Voltage Mode [A01]=[1]		1.8		
Feedback Resistor	Rf			200		KΩ
Driving Resistor	Rd	40MHz Mode [A18:A17]=[00]		1000		Ω
		40MHz Mode [A18:A17]=[01]		500		
		40MHz Mode [A18:A17]=[10]		250		
		40MHz Mode [A18:A17]=[11]		125		
Oscillating Capacitor	Cg/Cd	Offset Center [A11:A04]=[00000000]		4/4		pF
		Offset Max. [A11:A04]=[01111111]		2/2		
		Offset Min. [A11:A04]=[10000000]		6/6		

*The above values are the design values and are not guaranteed by test.



IC Block Diagram



Oscillator Block

Fig. 6-1 Block Diagram

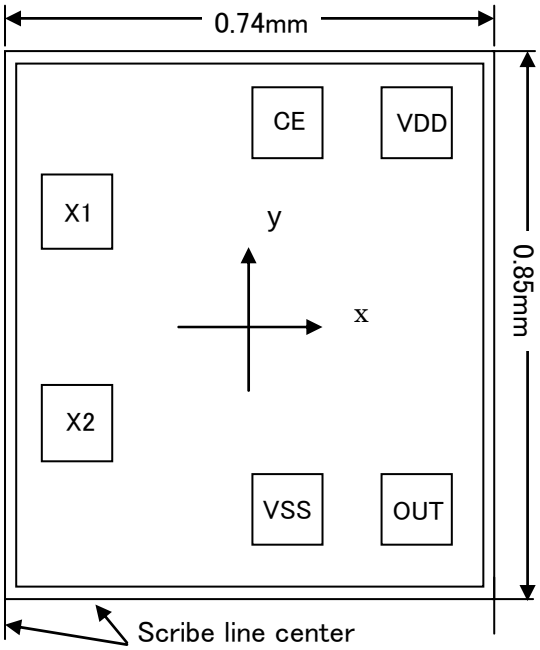
7. Compensation Parameters

$F(T) = \alpha(T - Ti)^3 + (T - Ti)\beta + \gamma$

Name	Bit	Digit	Range	Remarks
α	3	8	$100*10^{-6}\pm10\%$ ppm/°C^3	
β	4	16	−0.05～−0.40 ppm/°C	
γ	8	256	±30 ppm	～0.3 ppm/digit
Ti	5	32	27±16 °C	Including IC deviation

* The above value is just reference for crystal selection.
* These value depends on the sensitivity of the crystal.
* The above value corresponds to the crystal whose C0/C1≒300.

8. Pad Layout



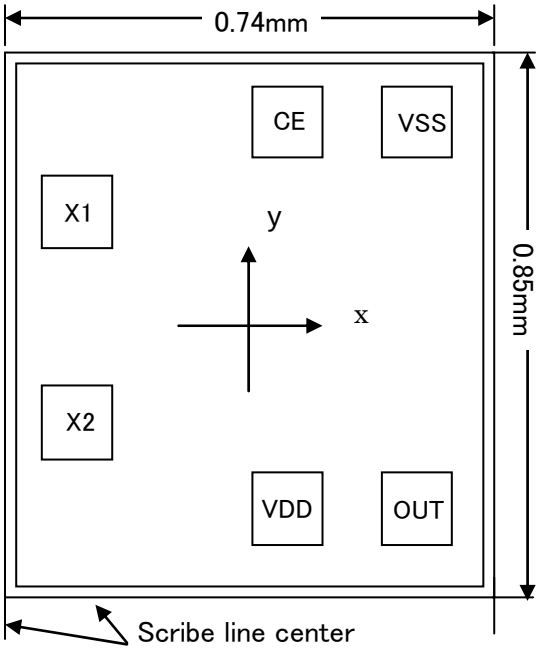
- Die Size : 0.74mm × 0.85mm
- Pad Size : 80um □
- Thickness : 150±20um
- IC Backside : Gnd or Open
- Scribe Line : 100um

Pad Name	Function	Location (μm)	
		x	y
VDD	(+)Power Supply	251	306
OUT(Q)	Frequency Output	251	−306
VSS	(−)Ground	83	−306
X2	Crystal Drive	−251	−137
X1	Crystal Feedback	−251	137
CE	Oscillation stop, "L": High-Impedance	83	306
Chip Center		0	0

Program mode

OUT(Q)	Clock
VDD	Mode Select
CE	ADIO : Digital input/Output and DC

Fig. 8-1 Cross Type



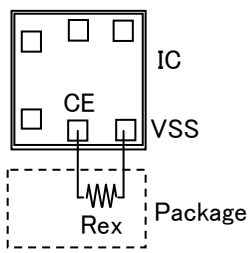
- Die Size : 0.74mm × 0.85mm
- Pad Size : 80um □
- Thickness : 150±20um
- IC Backside : Gnd or Open
- Scribe Line : 100um

Pad Name	Function	Location (μm)	
		x	y
VSS	(−)Ground	251	306
OUT(Q)	Frequency Output	251	−306
VDD	(+)Power Supply	83	−306
X2	Crystal Drive	−251	−137
X1	Crystal Feedback	−251	137
CE	Oscillation stop, "L": High-Impedance	83	306
Chip Center		0	0

Program mode

OUT(Q)	Clock
VDD	Mode Select
CE	ADIO : Digital input/Output and DC

Fig. 8-2 Flip Chip Type



IMPORTANT Notice for CE function

* Rex should be over 10MΩ in case of CE = Open usage.
* Oscillation will not be activated when CE = Open after CE = Low if Rex is below 10MΩ.
* There is no such issue in case of CE = VDD usage.
  Rex : External resistance value between CE and VSS of package.