■ Description

IPS050 is the specific SPXO IC for achieving low power KHz and low MHz range output by divide. The power consumption of IPS050 is quite low, and comparable with tuning fork solution.

■ Features

- Power consumption : 10uA typical with 512 divide
- Divide function : 1/256 ~ 1/1024 for KHz out, 1/4 ~ 1/16 for MHz out
- Output frequency : 27.344~52.734KHz, 54.688~105.469KHz / 0.31MHz ~ 8.5MHz
- Operation temperature : -40℃~85℃
- Power supply voltage : 1.6～3.63V
- Standby function : Oscillation stop
- Output : CMOS
- Small chip size : 0.52mm × 0.56mm
- Frequency stability to Vdd : Within ±1ppm

1. Part number rule

IPS 050 x M z B X -W 0

Series Name for SPXO

Product Series

Frequency

Mode	x	Frequency
Fundamental	3	5～34MHz

VDD
M : 1.6
～3.63V

Oscillation Mode & Divide

z	Mode	Divide
2	Funda mental	1/4
3		1/8
4		1/16
8		1/256
9		1/512
A		1/1024

z : $1/2^z$

Blank : Lower Idd
B : Depper NR

Pad Layout
X : Cross
F : Flip Chip

IC Form	Thickness	Definition
-W	0	Wafer 100um
Blank or -C	Blank	Chip 130um

2. Series

- Applicable crystal : AT Cut 8.39MHz, 14~27MHz and 33.55MHz for KHz output
  : AT Cut 5～34MHz for MHz output
- Power consumption : **Ultra Low Power consumption (10uA Typ) with KHz out**

Part Number	Crystal Frequency (MHz) Min.	Crystal Frequency (MHz) Max.	Divide	Output Frequency (KHz) Min.	Output Frequency (KHz) Max.	Pad Layout	Vdd (V)	Remarks
IPS050 3 M 8 X	8.388		1/256	32.768KHz		Cross	1.6 ～ 3.63	Lower Idd
IPS050 3 M 9 X	16.777		1/512					
IPS050 3 M A X	33.554		1/1024					
IPS050 3 M 8 B X	8.388	27.000	1/256	32.768	105.469			Deeper NR
IPS050 3 M 9 B X	14.000	27.000	1/512	27.344	52.734			
IPS050 3 M A B X	33.554		1/1024	32.768KHz				
IPS050 3 M 9 F	16.777		1/512	32.768KHz		Flip Chip		Lower Idd
IPS050 3 M A F	33.554		1/1024					
IPS050 3 M 9 B F	14.000	27.000	1/512	27.344	52.734			Deeper NR
IPS050 3 M A B F	33.554		1/1024	32.768KHz				
Part Number	MHz		Divide	MHz				
IPS050 3 M 2 X	5.00	34.00	1/4	1.25	8.50	Cross	1.6 ～ 3.63	Lower Idd
IPS050 3 M 3 X			1/8	0.63	4.25			
IPS050 3 M 4 X			1/16	0.31	2.13			

3. Absolute Maximum Ratings Unless otherwise stated, V_{SS}=0V, Ta=25℃±2℃

Parameter	Symbol	Condition	Ratings Min	Ratings Max	Ratings Unit
Supply Voltage	V_{DD}		V_{SS}-0.5	5.0	V
Input Voltage	V_{IN}	All Input Pin	V_{SS}-0.5	V_{DD}+0.5	V
Output Voltage	V_{OUT}		V_{SS}-0.5	V_{DD}+0.5	V
Input Current	I_{IN}	CE Pin		50	μA
Output Current	I_{OUT}			25	mA
Junction Temperature	Tj		-55	150	℃
Storage Temperature	T_{stg}		-55	125	℃

4. Recommended Operating Condition Unless otherwise stated, V_{SS}=0V, T a =- 40℃～+85℃

Parameter	Symbol	Condition	Min	Typ	Max	Unit	Note
Supply Voltage	V_{DD}		1.6		3.63	V	V_{DD}
“H” Input Voltage	V_{IH}		V_{DD}×0.7			V	CE
“L” Input Voltage	V_{IL}				V_{DD}×0.3	V	CE
Input Voltage	V_{IN}		V_{SS}		V_{DD}	V	CE
Output Load Capacitance	CL	CMOS			15	pF	OUT
Ambient Temperature	T_{opt}		-40		85	℃	

5. Electrical Specification

Unless otherwise stated, V_{DD}=3.3V, V_{SS}=0V, CL=15pF, T a =- 40℃～+85℃

Parameter		Symbol	Condition	Specification			Unit
				Min	Typ	Max	
Out put Leak current		Iz	CE=0V, X1=1.6V, Vss, Vout=Vss～VDD			10	μA
"H" input voltage		V_{IH}	CE pad	0.7V_{DD}			V
"L" input voltage		V_{IL}	CE pad			0.3V_{DD}	V
"H" input current		I_{IH}	CE pad, V_{IH}=V_{DD}			1	μA
"L" input current		I_{IL}	CE pad, V_{IL}=0V	-3			
Oscillation Disable Time		Tplz	OUT pad			0.1	μs
Oscillation Enable Time	IPS0503Mx	Tpzl	OUT pad			20	ms
Oscillation start up time	IPS0503Mx	Tstart	f_{xtal}=16MHz V_{DD}>1.6V			20	ms
"H" output voltage		V_{OH}	OUT pad, I_{OH}=-1.0mA	0.9V_{DD}			V
"L" output voltage		V_{OL}	OUT pad, I_{OL}=1.0mA			0.1V_{DD}	
Current consumption		I_{DD}	CL=15pF, VDD=3.3V, CE≧VDD-0.3V				μA
			IPS0503M8		10	15	
			IPS0503M9		10	15	
			IPS0503MA		18	27	
			IPS0503M8B, f_{xtal}=16MHz		20	30	
			IPS0503M9B, f_{xtal}=16MHz		20	30	
			IPS0503MAB		28	42	
			IPS0503M2 fxtal=12MHz		200	250	
			IPS0503M3 fxtal=19.2MHz		170	200	
			IPS0503M4 fxtal=33MHz		160	220	
Current consumption at oscillation disable		I_{DDD}	CL=15pF, VDD=3.3V, CE≦0.3V			3	μA
Frequency V_{DD} deviation		Fvst	V_{DD}=3.3±10%			±1	ppm
Output Duty Ratio		Duty	IPS0503M8, 9, A, xB	45		55	%
			IPS0503M2 fxtal=5~12MHz VDD=2.25~3.63V	45		55	%
			IPS0503M3 fxtal=5~24MHz VDD=2.25~3.63V	45		55	%
			IPS0503M4 fxtal=5~34MHz VDD=2.25~3.63V	45		55	%
			IPS0503M2, 3, 4 Except above condition	40		60	%
Rise/Fall time		Tr/Tf	10～90%VDD Except below			15.0	ns
			10～90%VDD IPS0503M3 VDD=2.7~3.3V			12.0	

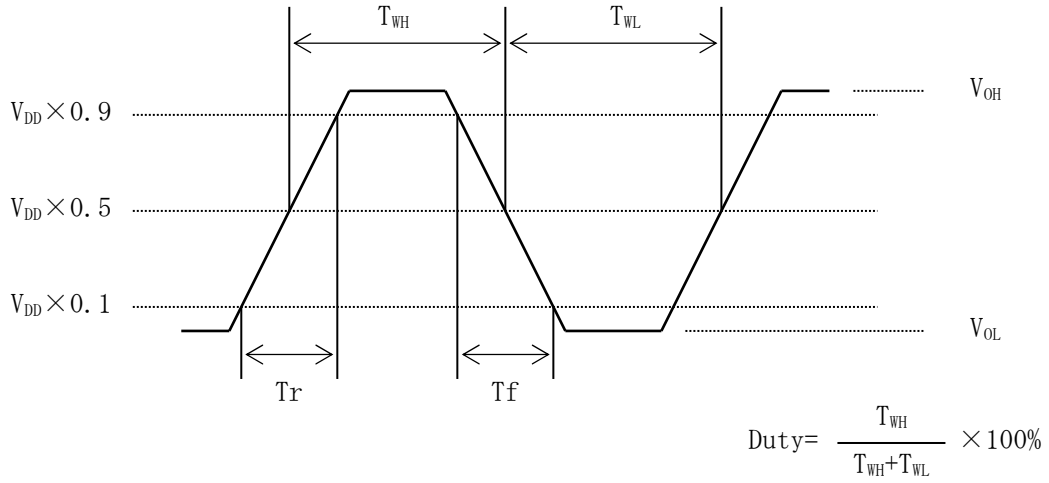
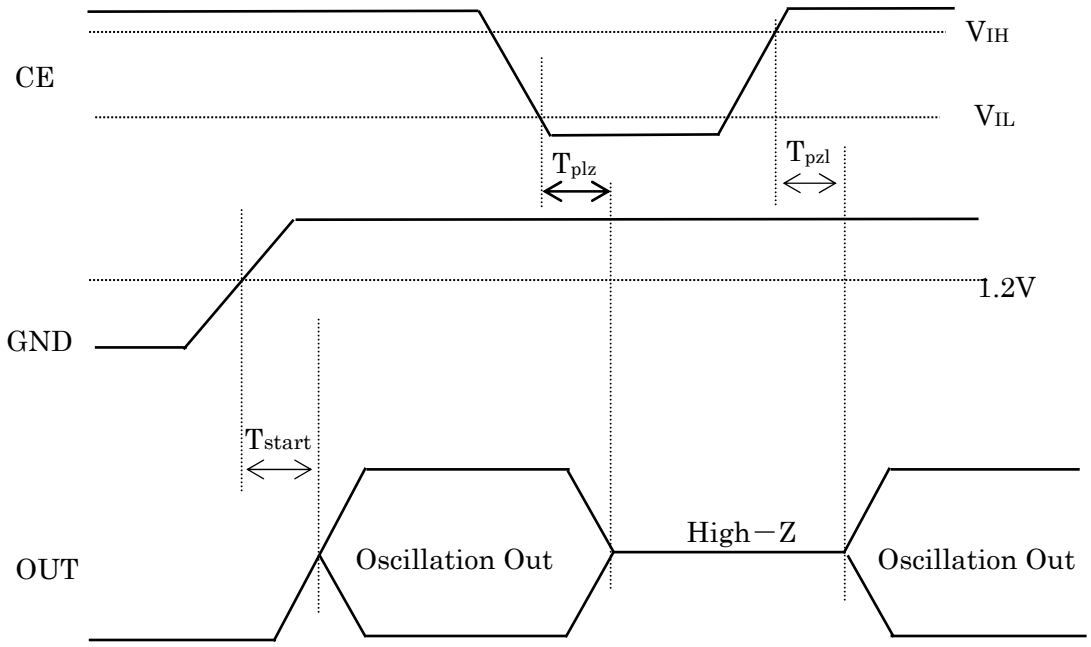


Fig. 5-1 Output wave form (Duty, Tr, Tf, V_{OH}, V_{OL})



V_{IH} : Threshold voltage for Oscillation Start
V_{IL} : Threshold voltage for Oscillation Stop

Fig. 5-2 Input output signal timing

6. Circuit Parameters of Oscillator (Reference Data for Circuit Design)

Ta=25℃, V_{DD}=3.3V

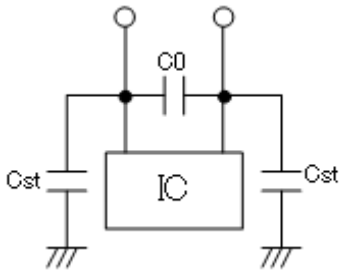
Parameter		Symbol	Condition	Typical value	Unit
Constant voltage output		Vreg	VDD=1.60V~3.63V	0.78	V
Feedback Resistor		Rf		348	KΩ
Driving Resistor		Rd		1000	Ω
Internal capacitor	IPS0503M8 IPS0503M9 IPS0503MA	Cg	Gate side	5.0	pF
	IPS0503MxB IPS0503M2 IPS0503M3 IPS0503M4			2.0	pF
		Cd	Drain side	2.0	pF

Ta=25℃, V_{DD}=3.3V

Parameter	Symbol	Condition		Frequency MHz	-Rs Ω
Negative resistance (Typical)	-Rs	C0=1.5pF Cst=1.0pF	IPS0503M9	17	-232
			IPS0503M8B	17	-578
			IPS0503M9B	17	-578
			IPS0503MAB	34	-201
			IPS0503M2, 3, 4	5	-4744
			IPS0503M2, 3, 4	34	-145

* The above values are the design values and are not guaranteed by test.

* Negative resistance was calculated using S parameters determined by network measurement under the estimation of crystal C0=1.5pF and Cst=1.0pF (Stray capacitance of SMD package). Refer the right side drawing as for C0 and Cst.



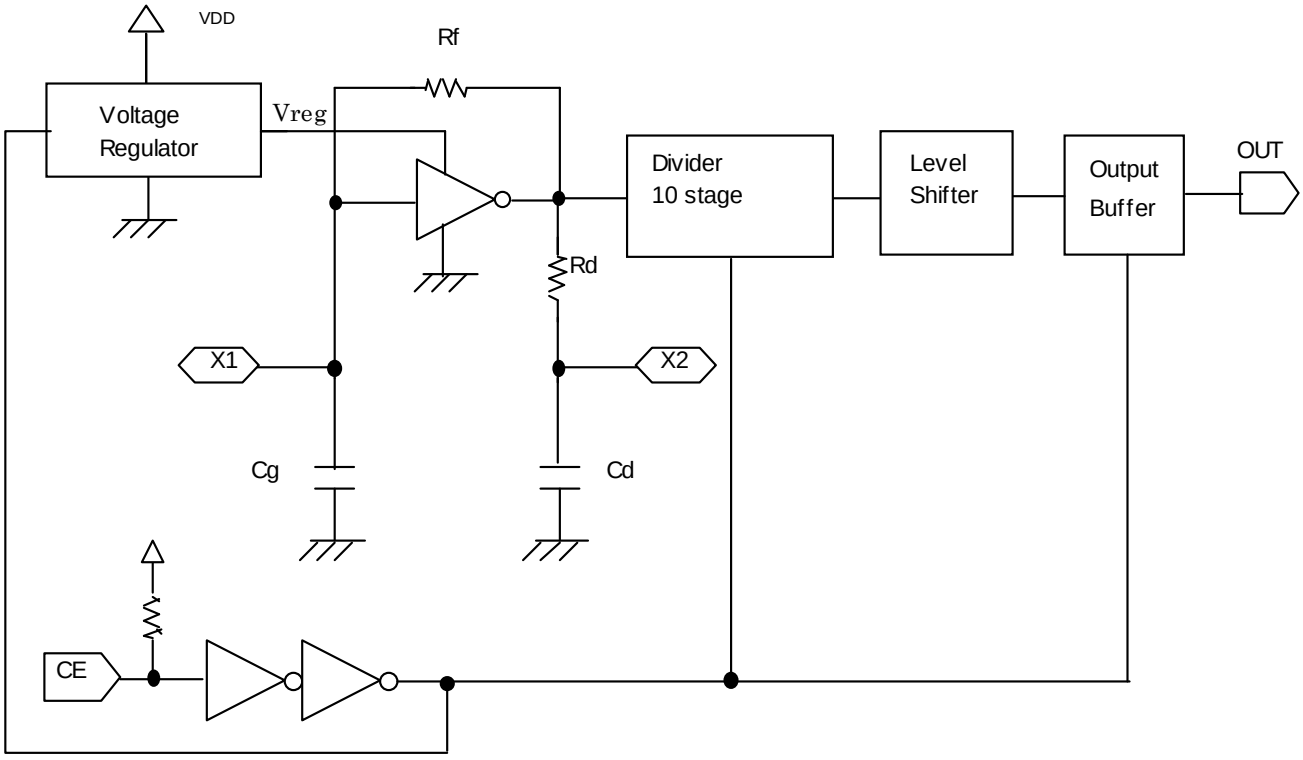
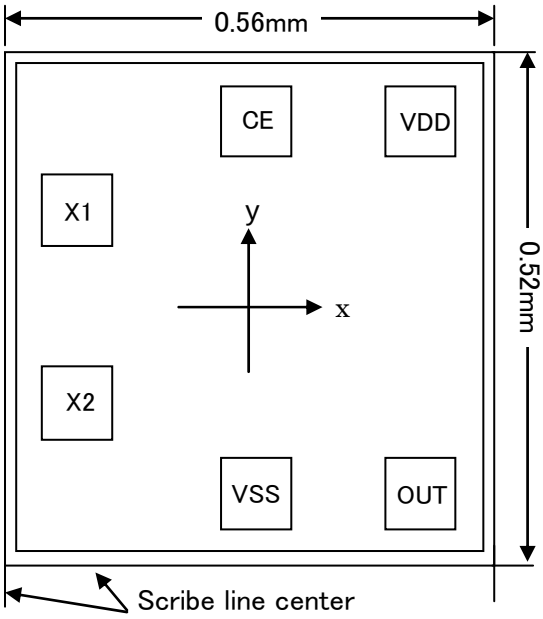


Fig. 6 Block Diagram

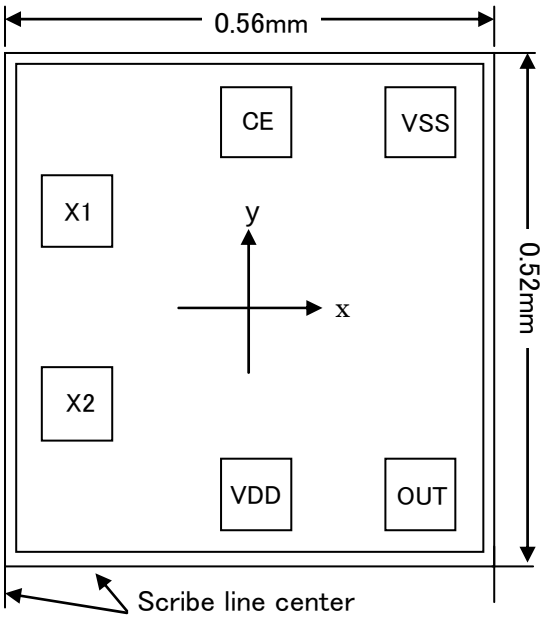
7. Pad Layout



- Die Size : 0.52mm × 0.56mm
- Pad Size : 80um □
- Thickness : 130±10um
- IC Backside : Gnd or Open
- Scribe Line : 80um

Pad Name	Function	Location (μm)	
		x	y
VDD	(+)Power Supply	175	155
OUT(Q)	Frequency Output	175	−155
VSS	(−)Ground	12	−155
X2	Crystal Drive	−175	−93
X1	Crystal Feedback	−175	93
CE	Oscillation stop, "L": High-Impedance	12	155
Chip Center		0	0

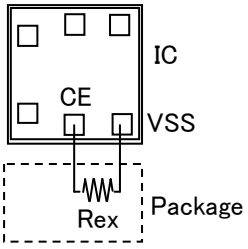
Fig. 7-1 Pad Layout of IPS050 (Cross Type)



- Die Size : 0.52mm × 0.56mm
- Pad Size : 80um □
- Thickness : 100±10um
- IC Backside : Gnd or Open
- Scribe Line : 80um

Pad Name	Function	Location (μm)	
		x	y
VSS	(−)Ground	175	155
OUT(Q)	Frequency Output	175	−155
VDD	(+)Power Supply	12	−155
X2	Crystal Drive	−175	−93
X1	Crystal Feedback	−175	93
CE	Oscillation stop, "L": High-Impedance	12	155
Chip Center		0	0

Fig. 7-2 Pad Layout of IPS050 (Flip Chip Type)



IMPORTANT Notice for CE function

* Rex should be over 10MΩ in case of CE = Open usage.
* Oscillation will not be activated when CE = Open after CE = Low if Rex is below 10MΩ.
* There is no such issue in case of CE = VDD usage.
  Rex : External resistance value between CE and VSS of package.