■ Description

IPS009BM is the specific SPXO IC for achieving low Phase Noise, corresponding to the fundamental crystal from 14MHz to 60MHz.

Both the operation temperature (-40℃~125℃) and V_{DD} range(1.62V~5.5V) is wide, so IPS009BM makes the selection of application wider.

■ Features

- Phase Noise : -165dBc/Hz @ 1MHz, V_{DD}=3.3V, F0=27MHz
- Phase Jitter : 102fs @ 12kHz~20MHz, V_{DD}=3.3V, F0=27MHz
- Operation temperature : -40℃~125℃
- Power supply voltage : 1.62V~5.5V
- Standby function : Oscillation stop
- Frequency Range : 14MHz ~ 60MHz
- Output : CMOS
- Divide function : 1/2, 1/4 and 1/8
- Small chip size : 0.70mm × 0.75mm
- Frequency stability to V_{DD} : Within ±1ppm
- Duty cycle : Within 50%±5%

1. Part number rule

IPS 009 B M z －C3 －W 1

- IPS: Series Name For SPXO
- 009: Product Series
- B: Crystal Frequency Range 14MHz～60MHz
- M: V_{DD} 1.62V~5.5V
- z: Divide Function
  - 0 : 1/1
  - 1 : 1/2 Divide
  - 2 : 1/4 Divide
  - 3 : 1/8 Divide
- －C3: Pad Layout C3 : Cross Type
- －W / 1:

IC Form	Thickness	Definition
－W	0	Wafer 100um
	1	Wafer 150um
Blank or －C	Blank	Chip 150um

2. Series

Part Number	Crystal Frequency f (MHz)		Divide	Output Frequency F0 (MHz)		Pad Layout	Remarks
	Min.	Max.		Min.	Max.		
IPS009 B M 0 -C3	14.00	60.00	1/1	14.00	60.00	Cross	
IPS009 B M 1 -C3			1/2	7.00	30.00		
IPS009 B M 2 -C3			1/4	3.50	15.00		
IPS009 B M 3 -C3			1/8	1.75	7.50		

3. Absolute Maximum Ratings

Vss=0V, Ta=25℃±2℃

Parameter	Symbol	Condition	Ratings		Unit
			Min	Max	
Supply Voltage	V_{DD}		V_{SS}-0.5	7.0	V
Input Voltage	V_{IN}	All Input Pin	V_{SS}-0.5	V_{DD}+0.5	V
Output Voltage	V_{OUT}		V_{SS}-0.5	V_{DD}+0.5	V
Output Current	I_{OUT}			25	mA
Junction Temperature	Tj		-55	150	℃
Storage Temperature	Tstg		-55	125	℃

4. Recommended Operating Condition

V_{SS}=0V, Ta=-40℃~125℃

Parameter	Symbol	Condition	Min	Typ	Max	Unit	Note
Supply Voltage	V_{DD}		1.62	3.3	5.5	V	V_{DD}
“H” Input Voltage	V_{IH}		V_{DD}×0.8			V	CE
“L” Input Voltage	V_{IL}				V_{DD}×0.2	V	CE
Input Voltage	V_{IN}		V_{SS}		V_{DD}	V	CE
Output Load Capacitance	CL	CMOS			15	pF	OUT
Ambient Temperature	Topt	Except below	-40		125	℃	
		V_{DD}=1.62~1.98V f=50MHz~60MHz	-40		85		

This IC has enough immunity against ESD and Latch-up, but handle with care.

5. Electrical Specification

Unless otherwise stated, V_{DD}=1.62V~5.5V, V_{SS}=0V, Ta=-40℃~125℃

Parameter	Symbol	Condition	Specification			Unit
			Min	Typ	Max	
Out put Leak current	Iz	CE=0V, X1=V_{DD} or Vss Vout=Vss~V_{DD}			15	μA
"H" input current	I_{IH}	CE pad, V_{IN}=V_{DD}	0		0.1	μA
"L" input current	I_{IL}	CE pad, V_{IN}=V_{SS}	-1.0		-0.01	μA
Output Disable Time	Tplz	OUT pad			0.1	μs
Output Enable Time	Tpzl	OUT pad			2.0	ms
Osc. start up time	Tstart	f=27MHz, V_{DD}≧1.62V			2.0	ms
"H" output voltage	V_{OH}	OUT pad, I_{OH}=-1.0mA	0.9V_{DD}			V
"L" output voltage	V_{OL}	OUT pad, I_{OL}=1.0mA			0.1V_{DD}	V
Current consumption	I_{DD}	CL=15pF, V_{DD}=1.8V CE≧V_{DD} -0.3V, f=27MHz		1.5	2.3	mA
		CL=15pF, V_{DD}=3.3V CE≧V_{DD} -0.3V, f=27MHz		2.8	4.2	
Current consumption at oscillation disable	I_{DDD}	V_{DD}=3.3V, CE≦0.3V		1.0	5.0	μA
Frequency V_{DD} deviation	Fvst	V_{DD}=5.0V±10%			±1.0	ppm
		V_{DD}=3.3V±10%			±1.0	
		V_{DD}=2.5V±10%			±1.0	
Duty Ratio	Duty	CL=15pF, 1/2V_{DD} point V_{DD}=1.62V~2.97V	40		60	%
		CL=15pF, 1/2V_{DD} point V_{DD}=2.97V~5.5V	45		55	
Rise/Fall time	Tr/Tf	CL=15pF, 10%~90%V_{DD} V_{DD}=1.62V~2.25V			6.5	ns
		CL=15pF, 10%~90%V_{DD} V_{DD}=2.25V~5.5V			4.0	

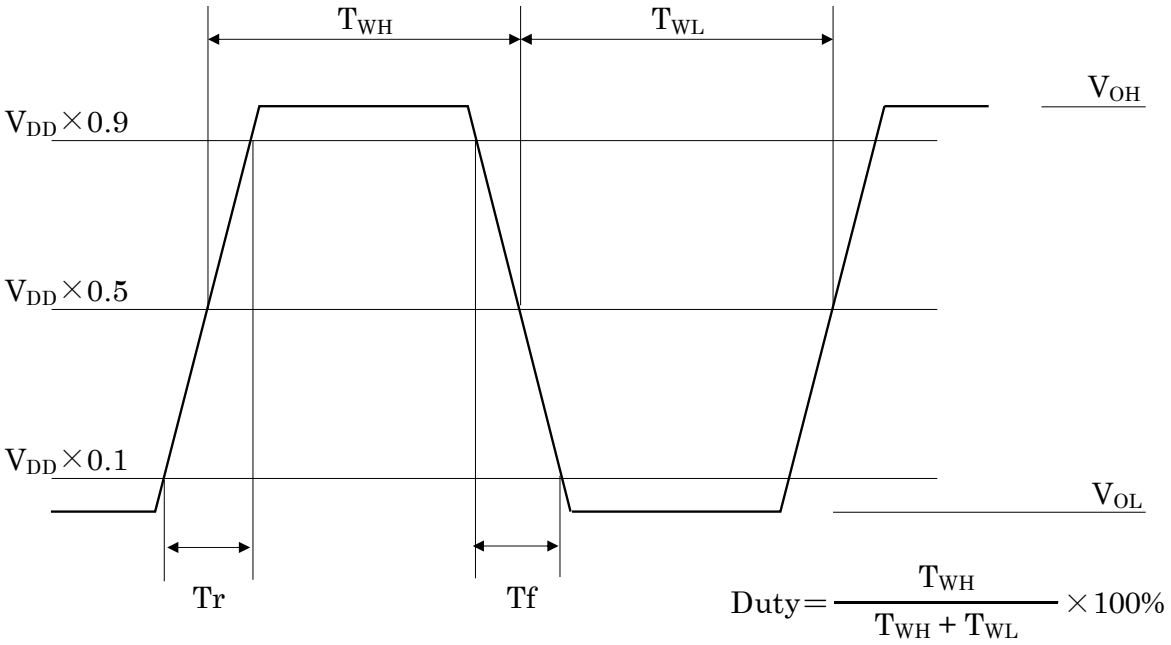
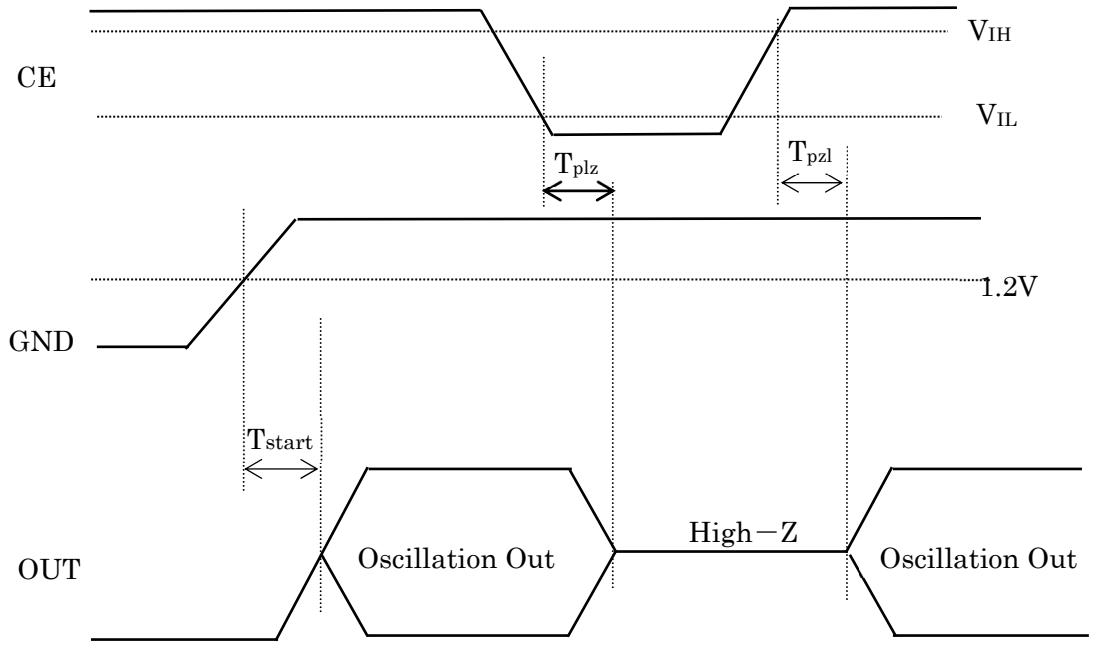


Fig. 5-1 Output wave form (Duty, Tr, Tf, V_{OH}, V_{OL})



V_{IH} : Threshold voltage for Oscillation Start
V_{IL} : Threshold voltage for Oscillation Stop

Fig. 5-2 Input output signal timing

6. Circuit Parameters of Oscillator (Reference Data for Circuit Design)

Ta=25℃

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Equivalent series (Loading) Capacitance	CLxtal	V_{DD}=2.7V, f=27MHz		6.0		pF
Drive Level	DL	V_{DD}=3.3V, f=27MHz		60		μW
Feedback Resistor	Rf			300		kΩ
Driving Resistor	Rd			1000		Ω
Oscillation Capacitor	Cg			8.0		pF
	Cd			12.0		

*The above values are the design values and are not guaranteed by test.

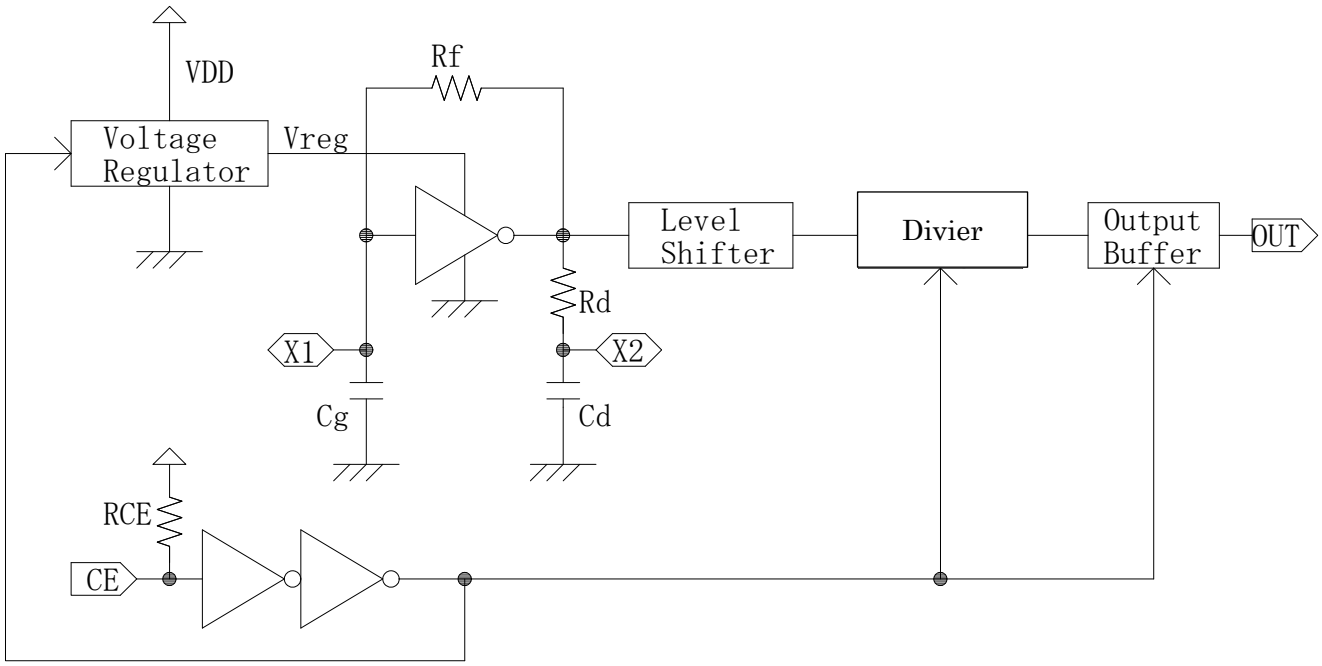
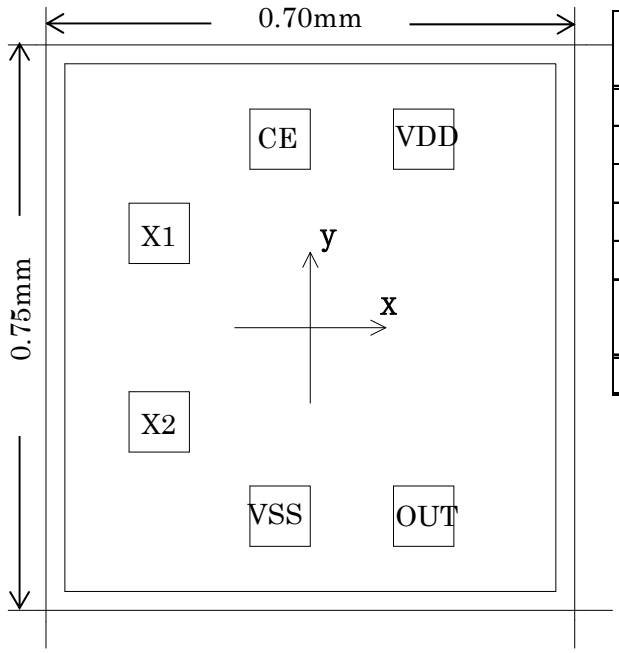


Fig. 6-1 Block Diagram

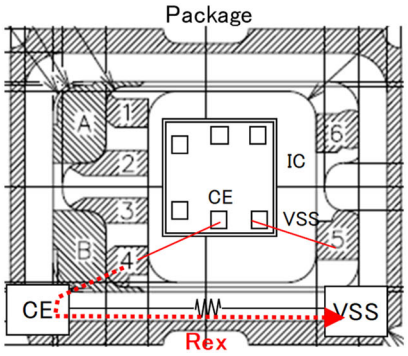
7. Pad Layout



Pad Name	Function	Location (μm)	
		x	y
VDD	(+) Power Supply	152	244
OUT(Q)	Frequency Output	152	-244
VSS	(−) Ground	-39	-244
X2	Crystal Drive	-209	-133
X1	Crystal Feedback	-209	133
CE	Oscillation stop "L": High-Impedance	-39	244
Chip Center		0	0

・Die Size：0.70mm × 0.75mm
・Pad Size：80um □
・Thickness：150um±20um
・IC Backside：Gnd or Open

Fig. 7-1 Pad Layout of IPS009BMz-C3



IMPORTANT Notice for CE function

※ Oscillation will not be activated when CE=Open after CE=Low if Rex is not large.
※ Reference value of Rex is over 10MΩ with CE=Open usage.
※ There is no such issue with CE=VDD usage.
Rex： Resistance value between CE and VSS of package