■ Description

The IPV045*L series is a VCXO IC that operates at low voltage and has a wide pull range. This IC contributes to the recent trend towards lower voltage and lower current consumption.

■ Features

- Operation temperature : -40℃~105℃
- Power supply voltage : 1.71V~1.89V
- Vc Input impedance : 5MΩ
- Standby function : Oscillation stop
- Crystal frequency : 24MHz~56MHz
- Output : CMOS
- Divide function : 1/2, 1/4 and 1/8
- Small chip size : 0.63mm × 0.75mm
- Frequency stability to V_{DD} : Within ±1ppm
- Wide pulling range : ±80ppm minimum / Vc=0.9V±0.9V
- Duty cycle : Within 50%±5%

1. Part number rule

IPV 045 x L z A －W 3

- IPV: Series Name For VCXO
- 045: Product Series
- x: Frequency Range

x	IPV045xLzA Frequency Range
2	24~40MHz
3	40~56MHz

- L: V_{DD}

Recommended V_{DD}	
L	1.8V

- z: Divide Function
  - 0: 1/1
  - 1: 1/2 Divide
  - 2: 1/4 Divide
  - 3: 1/8 Divide
- A: Optional code

Code	Definition
A	Lower Phase Noise version

- －W 3

IC Form	Thickness	Definition
－W	3	Wafer 130um
Blank or －C	Blank	Chip 130um

※Please contact us for wafer thickness.

2. Series

Part Number	Crystal Frequency f (MHz)		Divide	Output Frequency F0 (MHz)		Remarks
	Min.	Max.		Min.	Max.	
IPV045 2 L 0 A	24.00	40.00	1/1	24.00	40.00	Pad Layout : Straight
IPV045 2 L 1 A			1/2	12.00	20.00	
IPV045 2 L 2 A			1/4	6.00	10.00	
IPV045 2 L 3 A			1/8	3.00	5.00	
IPV045 3 L 0 A	40.00	56.00	1/1	40.00	56.00	
IPV045 3 L 1 A			1/2	20.00	28.00	
IPV045 3 L 2 A			1/4	10.00	14.00	
IPV045 3 L 3 A			1/8	5.00	7.00	

Please contact us for gray color models.

3. Absolute Maximum Ratings

V_{SS}=0V, Ta=25℃± 2℃

Parameter	Symbol	Condition	Ratings		
			Min	Max	Unit
Supply Voltage	V_{DD}		V_{SS}-0.5	5.0	V
Input Voltage	V_{IN}	All Input Pin	V_{SS}-0.5	V_{DD}+0.5	V
Output Voltage	V_{OUT}		V_{SS}-0.5	V_{DD}+0.5	V
Output Current	I_{OUT}			25	mA
Junction Temperature	Tj		-55	150	℃
Storage Temperature	Tstg		-55	125	℃

4. Recommended Operating Condition

V_{SS}=0V, Ta=-40℃~105℃(85℃)

Parameter	Symbol	Condition	Min	Typ	Max	Unit	Note
Supply Voltage	V_{DD}		1.71	1.80	1.89	V	V_{DD}
“H” Input Voltage	V_{IH}		V_{DD}×0.7			V	CE
“L” Input Voltage	V_{IL}				V_{DD}×0.3	V	CE
Input Voltage	V_{IN}		V_{SS}		V_{DD}	V	CE
Control Voltage	V_C		0		V_{DD}	V	VC
Output Load Capacitance	CL	CMOS			15	pF	OUT
Ambient Temperature	Topt		-40		105	℃	

This IC has enough immunity against ESD and Latch-up, but handle with care.

5. Electrical Specification

5-1 IPV0452LzA

Unless otherwise stated, V_{DD}=1.80V, V_{SS}=0V, Ta=-40℃~105℃

Parameter	Symbol	Condition		Specification			Unit
				Min	Typ	Max	
"H" input current	I_{IH}	$V_{IN}=V_{DD}$				10	μA
"L" input current	I_{IL}	$V_{IN}=V_{SS}$				1.0	μA
"H" output voltage	V_{OH}	I_{OH}=-1mA		V_{DD} ×0.9			V
"L" output voltage	V_{OL}	I_{OL}=1mA				V_{DD} ×0.1	V
Current consumption	I_{DD}	CL=15pF V_{DD}=1.8V Vc=0V f=30.72MHz	IPV0452L0A		2.0	4.0	mA
			IPV0452L1A		TBD		
			IPV0452L2A		TBD		
			IPV0452L3A		TBD		
Current consumption at oscillation stop	I_{DDD}	V_{DD}=1.8V、CE=GND				10	uA
Output off leak at oscillation stop	I_Z	CE≦0.3V				10	μA
Output Duty Ratio	Duty	CL=15pF, Vc=1/2V_{DD}		45		55	%
Pull Range	Fcntr	Vc=+0.9±0.9V 30.72MHz Crystal *1		±80	±100		ppm
Rise time	Tr	CL=15pF, 10%~90% V_{DD}				6.0	ns
Fall time	Tf	CL=15pF, 90%~10% V_{DD}				6.0	ns
Output Enable Time	Tpe					5.0	ms
Output Disable Time	Tpd					200	ns
Oscillation start up time	Tstart					5.0	ms
Modulation Band Width	Fc	Vc=0.9sinωt+0.9V, -3dB		10	15		kHz

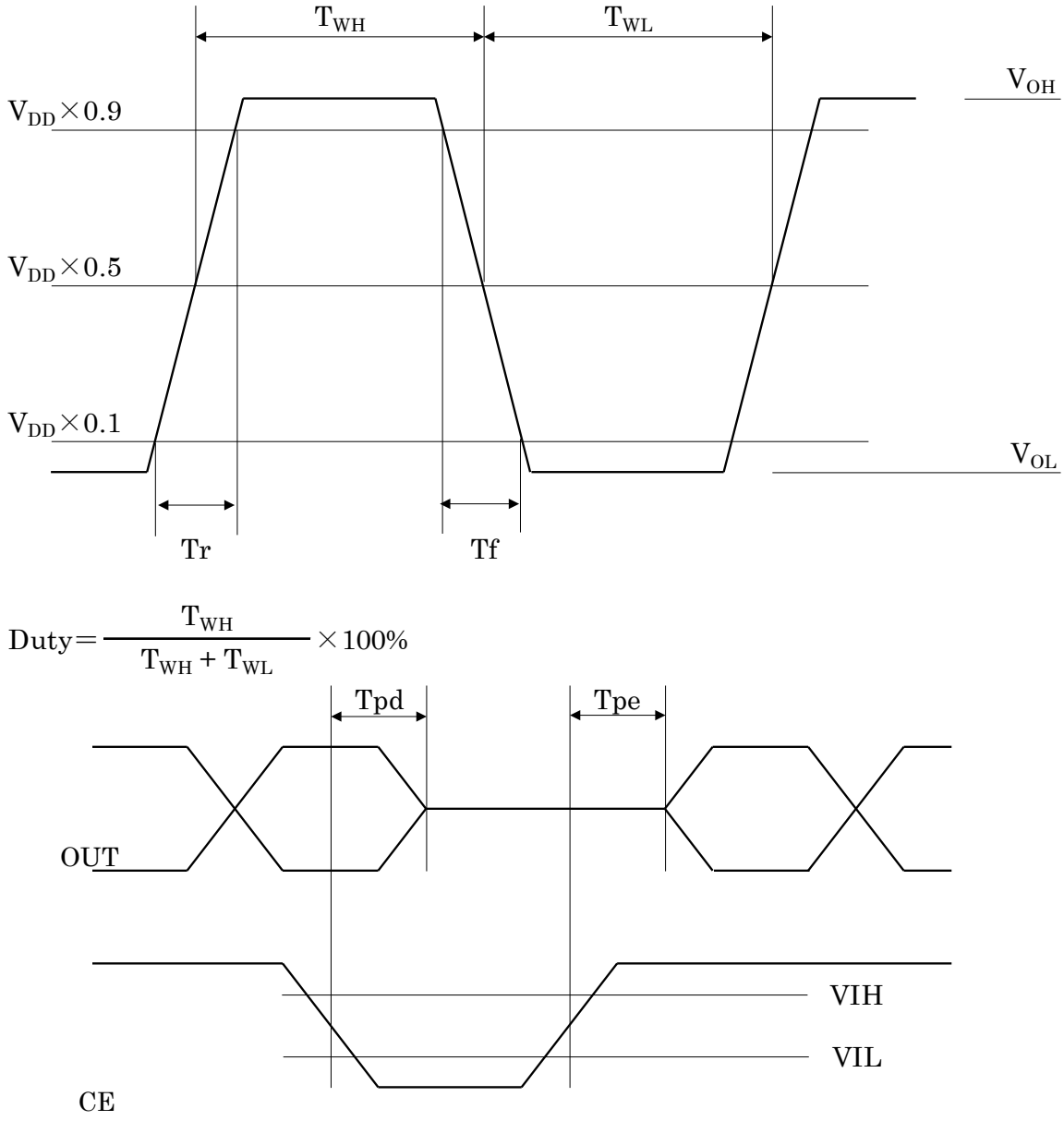
Crystal *1 ; Equivalent Parameter of Crystal is γ=C0/C1≒270

5-2 IPV0453LzA

Unless otherwise stated, V_{DD}=1.80V, V_{SS}=0V, Ta=-40℃~105℃

Parameter	Symbol	Condition		Specification			Unit
				Min	Typ	Max	
"H" input current	I_{IH}	V_{IN}=V_{DD}				10	μA
"L" input current	I_{IL}	V_{IN}=V_{SS}				1.0	μA
"H" output voltage	V_{OH}	I_{OH}=-1mA		V_{DD} ×0.9			V
"L" output voltage	V_{OL}	I_{OL}=1mA				V_{DD} ×0.1	V
Current consumption	I_{DD}	CL=15pF V_{DD}=1.8V Vc=0V f=54MHz	IPV0453L0A		3.5	7.0	mA
			IPV0453L1A		TBD		
			IPV0453L2A		TBD		
			IPV0453L3A		TBD		
Current consumption at oscillation stop	I_{DDD}	V_{DD}=1.8V、CE=GND				10	uA
Output off leak at oscillation stop	Iz	CE≦0.3V				10	μA
Output Duty Ratio	Duty	CL=15pF, Vc=1/2V_{DD}		45		55	%
Pull Range	Fcntr	Vc=+0.9±0.9V 54MHz Crystal *1		±80	±100		ppm
Rise time	Tr	CL=15pF, 10%~90% V_{DD}				4.0	ns
Fall time	Tf	CL=15pF, 90%~10% V_{DD}				4.0	ns
Output Enable Time	Tpe					5.0	ms
Output Disable Time	Tpd					200	ns
Oscillation start up time	Tstart					5.0	ms
Modulation Band Width	Fc	Vc=0.9sinωt+0.9V, -3dB		10	15		kHz

Crystal *1 ; Equivalent Parameter of Crystal is γ=C0/C1≒300



VIH : Threshold voltage for Oscillation Start
VIL : Threshold voltage for Oscillation Stop

Fig. 5-1 Output Wave Form (Duty, Tr, Tf, Tpd, Tpe)

6. Circuit Parameters of Oscillator (Reference Data for Circuit Design)

Ta=25℃, Vc= V_{SS}~V_{DD}

Parameter		Symbol	Condition	Min	Typ	Max	Unit
Feedback Resistor	IPV0452L0A	Rf	Refer to Fig. 6-1		180		kΩ
	Others				120		
Driving Resistor		Rd			1200		Ω
Bias Resistor		R_{V1}			240		kΩ
		R_{V2}			120		kΩ
Input Resistor		R_{VC}			40		kΩ
DC cut Capacitor		Cpg			15.0		pF
		Cpd			37.5		
VC Input impedance		Zvc	VC terminal to GND	5			MΩ

*The above values are the design values and are not guaranteed by test.

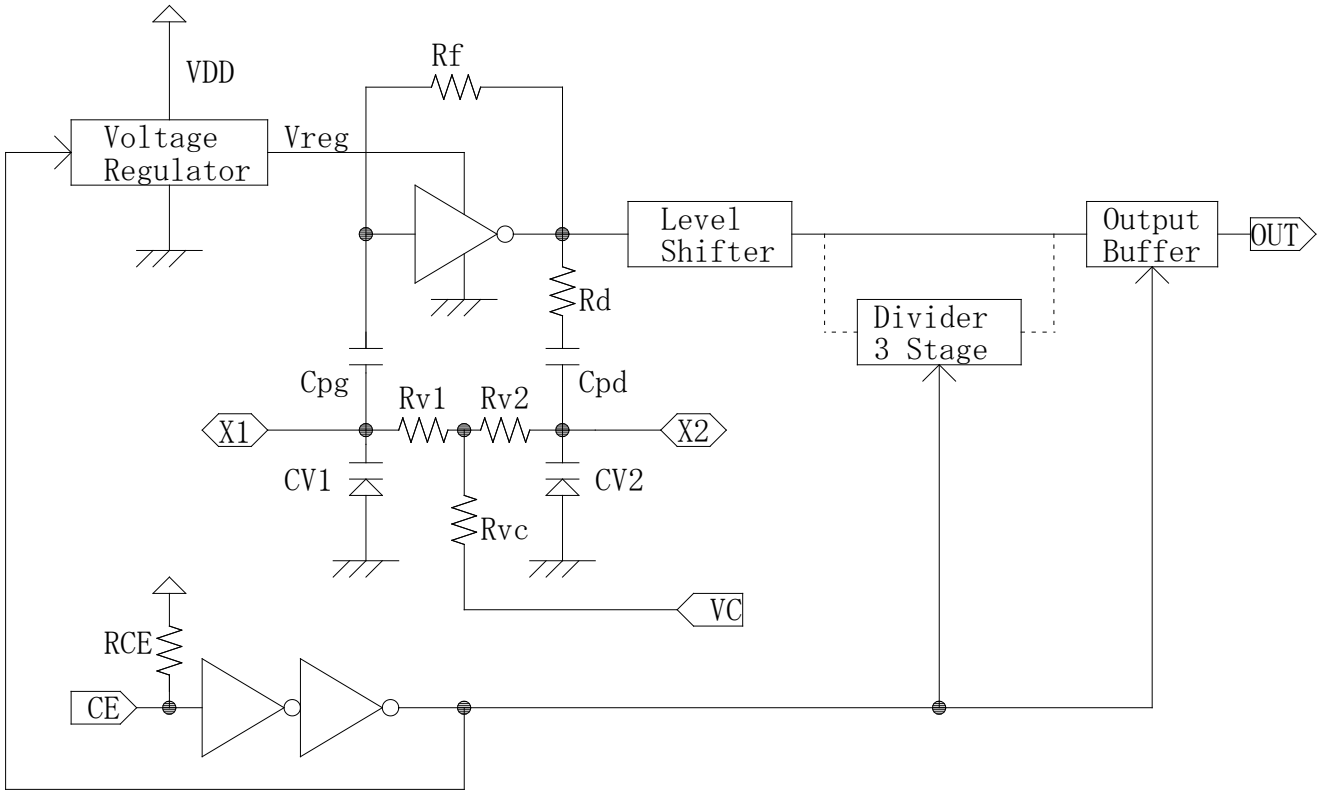
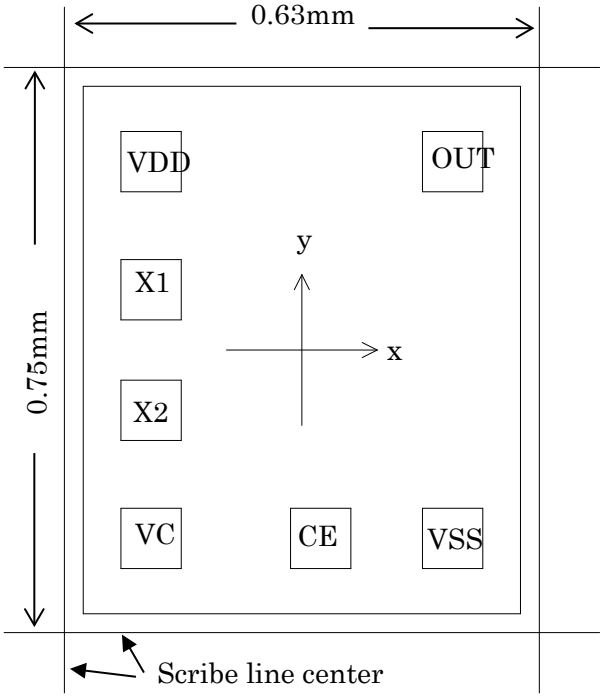


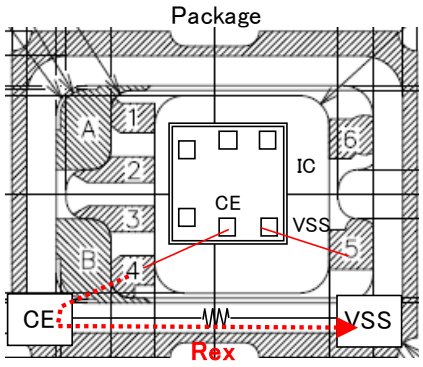
Fig. 6-1 Block Diagram

7. Pad Layout



- Die Size : 0.63mm × 0.75mm
- Pad Size : 80um □
- Thickness : 130um±10um
- IC Backside : Gnd or Open

Pad Name	Function	Location (μm)	
		x	y
VDD	(+) Power Supply	-196	256
X1	Crystal Feedback	-196	83
X2	Crystal Drive	-196	-83
VC	Frequency Control Input	-196	-256
CE	Oscillation stop "L": High-Impedance	28	-256
VSS	(−) Ground	196	-256
OUT	Frequency Output	196	256
Chip Center		0	0



IMPORTANT Notice for CE function

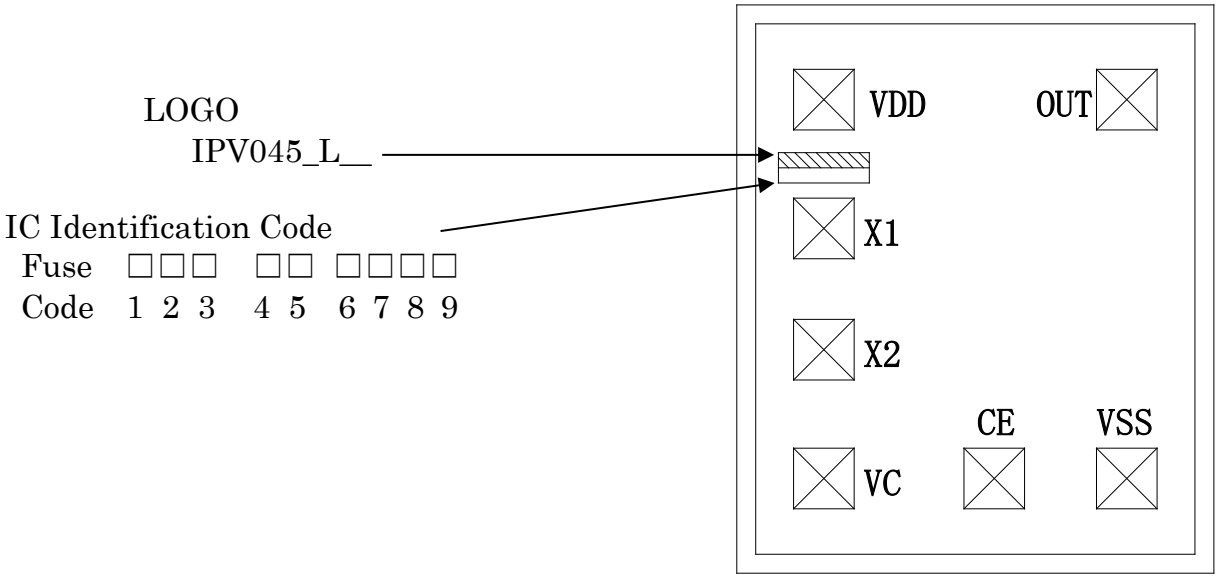
※ Oscillation will not be activated when CE=Open after CE=Low if Rex is not large.

※ Reference value of Rex is over 10MΩ with CE=Open usage.

※ There is no such issue with CE=VDD usage.

Rex： Resistance value between CE and VSS of package

8. IC Part # Identification



Part #	Code 1~9
IPV0452L0A	□■□ □□ □□□■
IPV0452L1A	□■□ □■ □□□■
IPV0452L2A	□■□ ■□ □□□■
IPV0452L3A	□■□ ■■ □□□■
IPV0453L0A	□■■ □□ □□□■
IPV0453L1A	□■■ □■ □□□■
IPV0453L2A	□■■ ■□ □□□■
IPV0453L3A	□■■ ■■ □□□■

□ : Fuse no cut

■ : Fuse cut

9. Revision History

Revision No.	Revision Date	Revised items	Before Revision	After Revision
VC-3.2	2025/11/04	Wafer thickness 100um	Listed	As requested
		IPV0453L2	Listed	Unlisted
		I_{DDD} Condition	CE=Low	CE=GND