

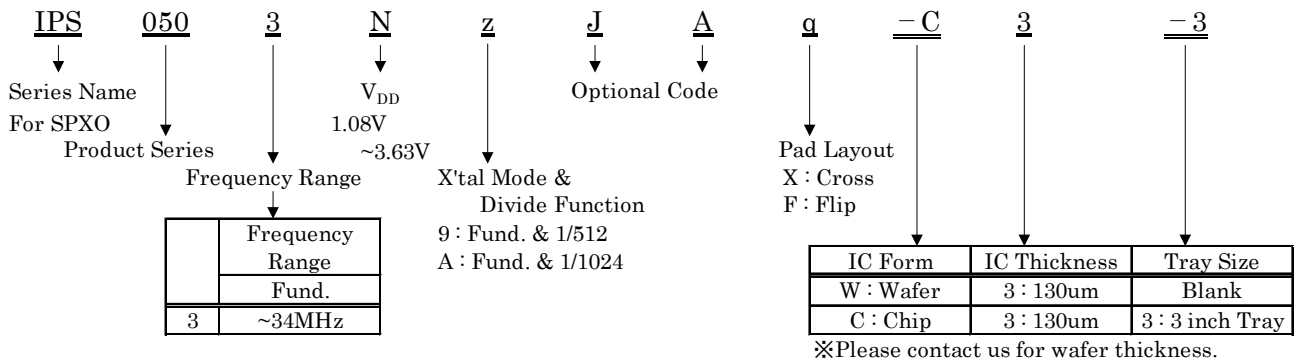
■ Description

IPS050*JA [kHz] series is the specific SPXO IC for achieving 32.768kHz output by divide. The power consumption of IPS050*JA [kHz] series is quite Low, and comparable with tuning fork solution.

■ Features

- Power consumption : 12μA typical (IPS0503NAJAq, V_{DD}=3.3V, No Load, Ta=25°C)
- Divide function : 1/512 and 1/1024
- Output frequency : 32.768kHz
- Operation temperature : -40°C~125°C
- Power supply voltage : 1.08V~3.63V
- Standby function : Oscillation stop
- Output : CMOS
- Small chip size : 0.55mm × 0.54mm
- Frequency stability to V_{DD} : Within ±1.0ppm

1. Part number rule



2. Series

Part Number						Crystal Frequency f (MHz)	Divide	Output Frequency F0 (kHz)	Pad Layout	Remarks
IPS050	3	N	9	J	A	X	16.777	1/512	Cross	
IPS050	3	N	A	J	A	X	33.554	1/1024		
IPS050	3	N	9	J	A	F	16.777	1/512	Flip	
IPS050	3	N	A	J	A	F	33.554	1/1024		

Please contact us for gray color models.

3. Absolute Maximum Ratings

Unless otherwise stated, $V_{SS}=0V$, $T_a=25^{\circ}C\pm 2^{\circ}C$

Parameter	Symbol	Condition	Ratings		
			Min	Max	Unit
Supply Voltage	V_{DD}		$V_{SS}-0.5$	5.0	V
Input Voltage	V_{IN}	Except below	$V_{SS}-0.5$	$V_{DD}+0.5$	V
		X1, X2	$V_{SS}-0.5$	2.0	
Output Voltage	V_{OUT}		$V_{SS}-0.5$	$V_{DD}+0.5$	V
Output Current	I_{OUT}			25	mA
Junction Temperature	T_j		-55	150	$^{\circ}C$
Storage Temperature	T_{stg}		-55	125	$^{\circ}C$

4. Recommended Operating Condition

Unless otherwise stated, $V_{SS}=0V$, $T_a=-40^{\circ}C\sim 125^{\circ}C$

Parameter	Symbol	Condition	Min	Typ	Max	Unit	Note
Supply Voltage	V_{DD}		1.08		3.63	V	V_{DD}
Input Voltage	V_{IN}		V_{SS}		V_{DD}	V	CE
Output Load Capacitance	CL	CMOS			15	pF	OUT
Ambient Temperature	T_{opt}		-40		125	$^{\circ}C$	

5. Electrical Specification

 Unless otherwise stated, $V_{DD}=1.08V\sim 3.63V$, $V_{SS}=0V$, $CL=15pF$, $T_a=-40^{\circ}C\sim 125^{\circ}C$

Parameter	Symbol	Condition	Specification			Unit
			Min	Typ	Max	
Output leak current	I_z	CE=0V, X1=2.0V or V_{SS} $V_{out}=V_{SS}\sim V_{DD}$			20	μA
“H” input voltage	V_{IH}	CE Pad	$0.8V_{DD}$			V
“L” input voltage	V_{IL}	CE Pad			$0.2V_{DD}$	V
“L” input current	I_{IL}	CE Pad, $V_{IL}=0V$		-10		μA
Oscillation Disable Time	T_{plz}	OUT Pad			0.2	μs
Oscillation Enable Time	T_{pzl}	OUT Pad			2.0	ms
Oscillation Start up Time	T_{start}	$V_{DD}=1.2V$			5.0	ms
		$V_{DD}=1.8V, V_{DD}=3.3V$			2.0	
“H” output voltage	V_{OH}	OUT Pad, $I_{OH}=-1.0mA$, $V_{DD}=3.3V$	$0.9V_{DD}$			V
“L” output voltage	V_{OL}	OUT Pad, $I_{OL}=1.0mA$, $V_{DD}=3.3V$			$0.1V_{DD}$	V
Current consumption	I_{DD}	$V_{DD}=1.2V$ No Load	IPS0503N9JA		14.5	μA
			IPS0503NAJA		26.0	
		$V_{DD}=1.8V$ No Load	IPS0503N9JA		14.5	
			IPS0503NAJA		26.0	
		$V_{DD}=3.3V$ No Load	IPS0503N9JA		15.0	
			IPS0503NAJA		27.0	
Current consumption at oscillation disable	I_{DDD}	$V_{DD}=3.3V$, CE=GND		0.6	3.0	μA
Freq. V_{DD} deviation	F_{VST}	$V_{DD}\pm 10\%$ ($V_{DD}=1.2V, 1.8V, 3.3V$)			± 1.0	ppm
Output Duty Ratio	Duty	$CL=15pF$, $1/2V_{DD}$ point	45		55	%
Rise time/Fall time	T_r/T_f	$CL=15pF$ $10\%\leftrightarrow 90\%V_{DD}$	$V_{DD}=1.2V$		30.0	ns
			$V_{DD}=1.8V$		15.0	
			$V_{DD}=3.3V$		7.5	

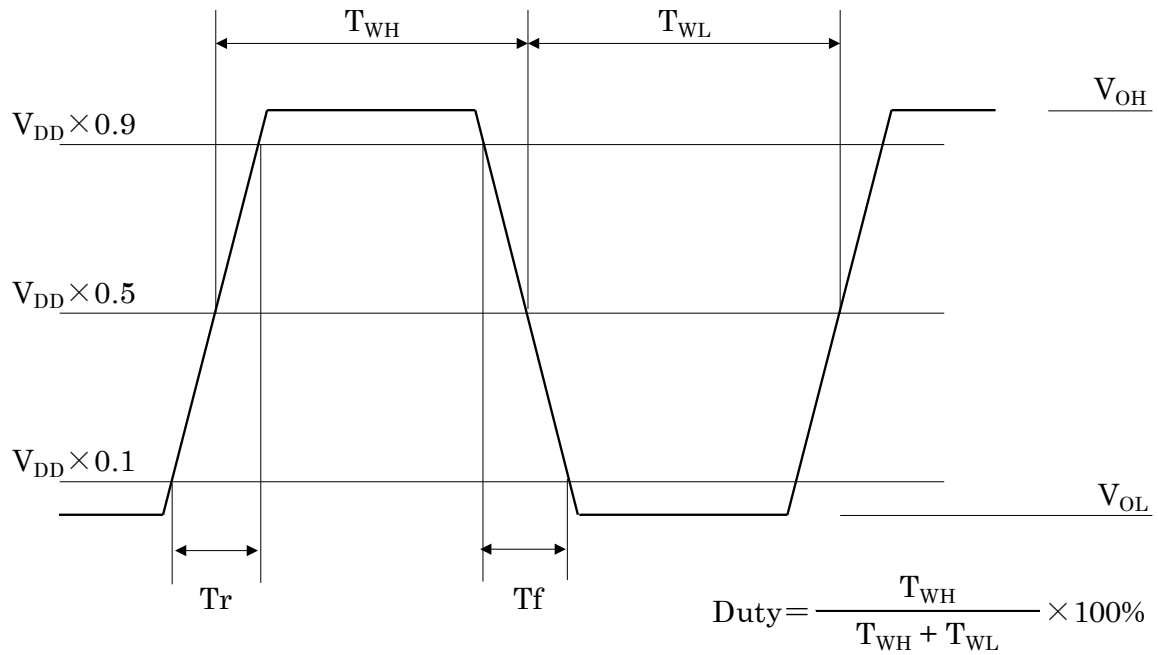
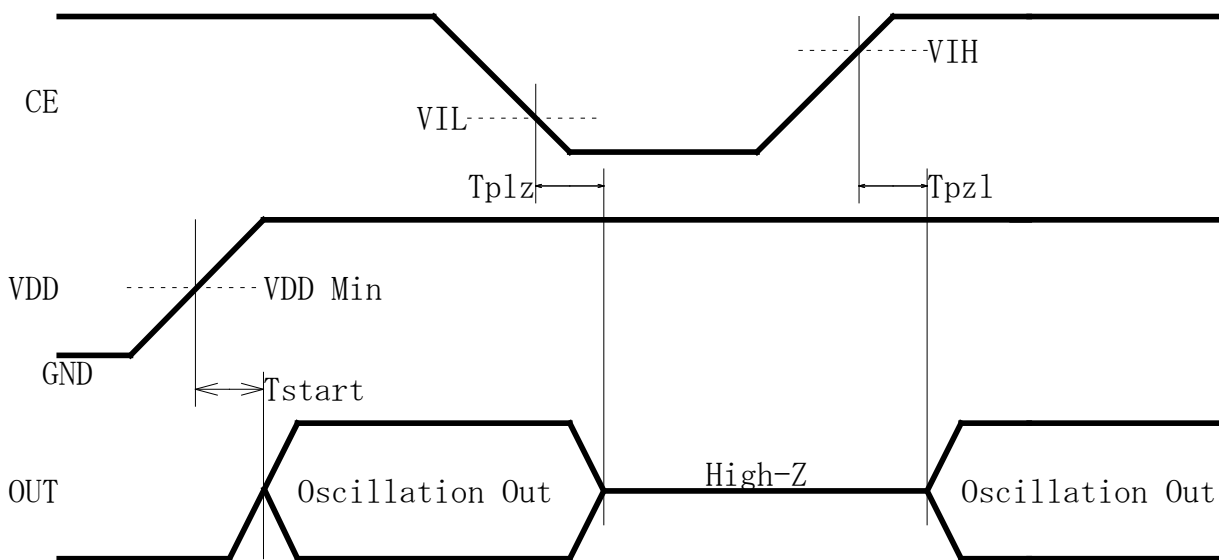


Fig. 5-1 Output wave form (Duty, Tr, Tf, VOH, VOL)



V_{IH} : Threshold voltage for Oscillation Start
 V_{IL} : Threshold voltage for Oscillation Stop

Fig. 5-2 Input output signal timing

6. Circuit Parameters of Oscillator (Reference Data for Circuit Design)
 $T_a=25^{\circ}\text{C}$

Parameter	Symbol	Condition	Typical value	Unit
Regulated Voltage	Vreg		0.8	V
Feedback Resistor	Rf		570	k Ω
Driving Resistor	Rd		1000	Ω
Oscillation Capacitor	Cg	Gate side	3.0	pF
	Cd	Drain side	1.0	pF

* The above values are the design values and are not guaranteed by test.

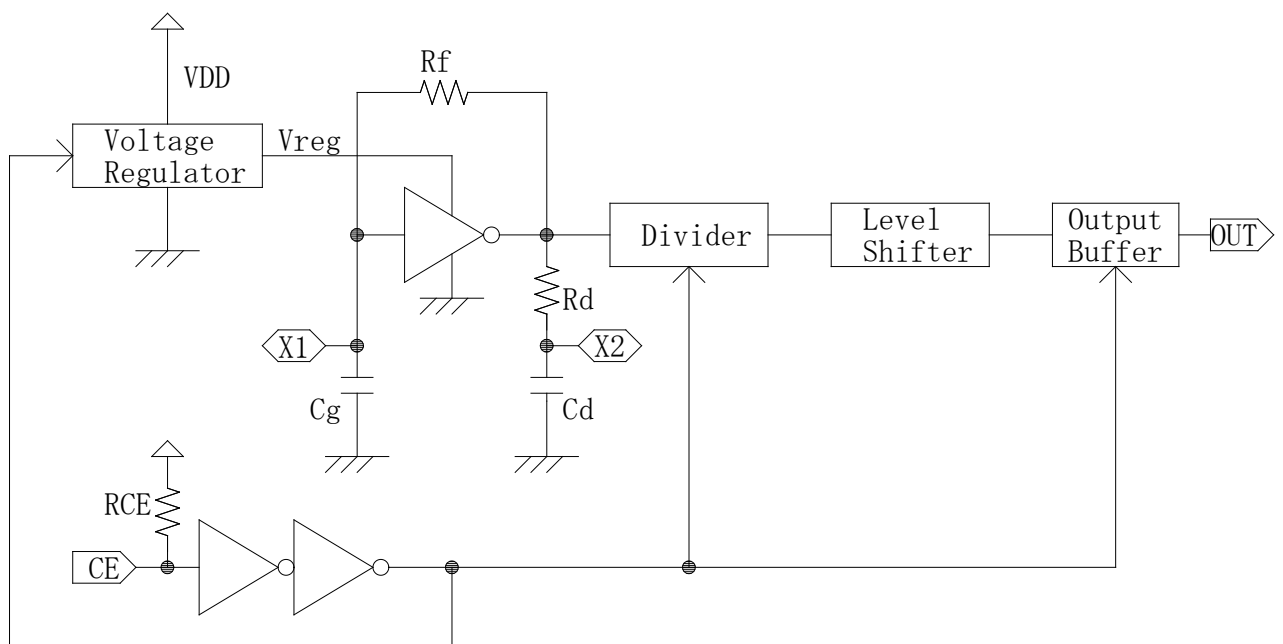
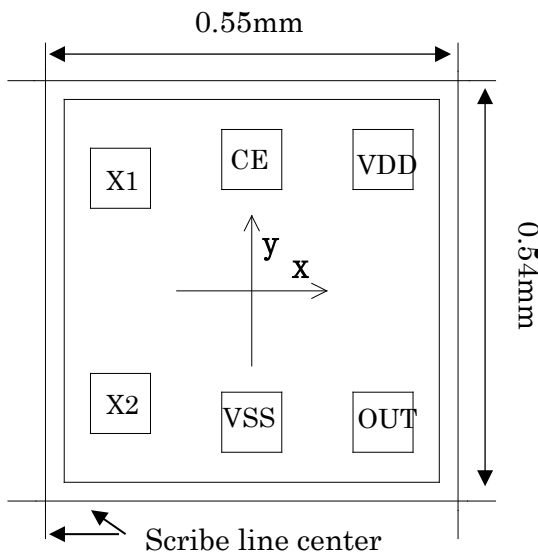


Fig. 6-1 Block Diagram

7. Pad Layout

7-1 Cross Type

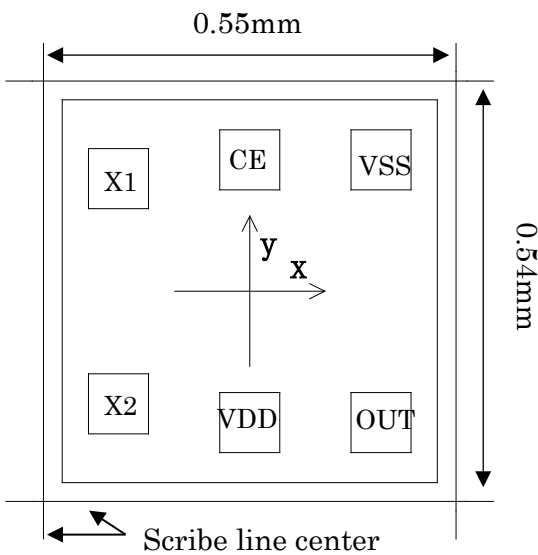


- Die Size: 0.55mm × 0.54mm
- Pad Size: 80um □
- Thickness: 130um±10um
- Scribe Line: 60um
- IC Backside: Gnd or Open

Pad Name	Function	Location (μm)	
		x	y
VDD	(+) Power Supply	180	175
OUT(Q)	Frequency Output	180	-175
VSS	(-) Ground	0	-175
X2	Crystal Drive	-180	-150
X1	Crystal Feedback	-180	150
CE	Oscillation stop "L": High-Impedance	0	175
Chip Center		0	0

Fig. 7-1 Pad Layout of IPS0503NzJAX

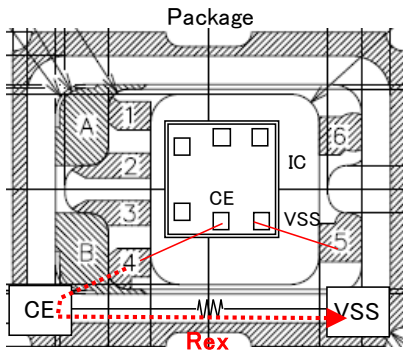
7-2 Flip Type



- Die Size: 0.55mm × 0.54mm
- Pad Size: 80um □
- Thickness: 130um±10um
- Scribe Line: 60um
- IC Backside: Gnd or Open

Pad Name	Function	Location (μm)	
		x	y
VSS	(-) Ground	180	175
OUT(Q)	Frequency Output	180	-175
VDD	(+) Power Supply	0	-175
X2	Crystal Drive	-180	-150
X1	Crystal Feedback	-180	150
CE	Oscillation stop "L": High-Impedance	0	175
Chip Center		0	0

Fig. 7-2 Pad Layout of IPS0503NzJAF



IMPORTANT Notice for CE function

- ※ Oscillation will not be activated when CE=Open after CE=Low if Rex is not large.
- ※ Reference value of Rex is over 10MΩ with CE=Open usage.
- ※ There is no such issue with CE=VDD usage.

Rex : Resistance value between CE and VSS of package

8. Revision History

Revision No.	Revision Date	Revised items	Before Revision	After Revision
SC-7.1	2025/11/04	1st edition	-	-
SC-7.2	2026/06/17	IPS0503N9JAX	Under Development	Listed
		IPS0503NAJAX	Under Development	Listed
		Current consumption IPS0503N9JA $V_{DD}=1.2V$ No Load	TBD	14.5uA