■ Description

IPS009 is the IC for SPXO corresponding to the fundamental crystal from 14MHZ to 100MHz, and operation voltage is 1.2V minimum, so it is the best for the application to the hand-held apparatus of a battery drive. The operation temperature is quite high (125℃), so IPS009 can be used for various applications.

■ Features

- Operation temperature : 125℃
- Power supply voltage : 1.2～3.63V / IPS009BL and 1.62～3.63V / IPS009CM
- Standby function : Oscillation stop
- Crystal frequency : 100MHz maximum
- Low power consumption : 1.2mA (IPS009BL)
- Output : CMOS
- Divide function : 1/2, 1/4 and 1/8
- Small chip size : 0.70mm × 0.75mm
- Frequency stability to Vdd : Within ±1ppm
- Duty cycle : Within 50±5%

1. Part number rule

IPS009B L z -C1

- IPS: Series Name for SPXO
- 009: Product Series
- B: Frequency Range
- L: VDD
- z: Divide Function
  - 0 : 1/1
  - 1 : 1/2 Divide
  - 2 : 1/4 Divide
  - 3 : 1/8 Divide
- -C1: Pad Layout
  - C1 : Straight
  - C2 : Cross

Conbination of Frequency and VDD	VDD (V)	
	L	M
Frequency Range	1.2～3.63	1.62～3.63
B : 14～48MHz	○	NA
C : 48～100MHz	NA	○

2. Series

Part Number	Output Frequency (MHz)		Divide	Pad Layout	Vdd (V)	Remarks
	Min.	Max.				
IPS009 B L 0 -C1	14.00	48.00	1/1	Straight	1.2 *1)～3.63	Low Vdd *1) 1.3V at 125℃
IPS009 B L 1 -C1	7.00	24.00	1/2			
IPS009 B L 2 -C1	3.50	12.00	1/4			
IPS009 B L 3 -C1	1.75	6.00	1/8			
IPS009 B L 0 -C2	14.00	48.00	1/1	Cross		
IPS009 C M 0 -C1	48.00	100.00	1/1	Straight	1.62～3.63	High Frequency
IPS009 C M 1 -C1	24.00	50.00	1/2			
IPS009 C M 2 -C1	12.00	25.00	1/4			
IPS009 C M 3 -C1	6.00	12.50	1/8			

3. Absolute Maximum Ratings Vss=0V, Ta=25℃±2℃

Parameter	Symbol	Condition	Ratings		
			Min	Max	Unit
Supply Voltage	V_{DD}		V_{SS}-0.5	7.0	V
Input Voltage	V_{IN}	All Input Pin	V_{SS}-0.5	V_{DD}+0.5	V
Output Voltage	V_{OUT}		V_{SS}-0.5	V_{DD}+0.5	V
Input Current	I_{IN}	CE Pin		50	μA
Output Current	I_{OUT}			25	mA
Junction Temperature	Tj		-55	150	℃
Storage Temperature	Tstg		-55	125	℃

4. Recommended Operating Condition V_{SS}=0V, T a =- 40℃～＋125℃

Parameter		Symbol	Condition	Min	Typ	Max	Unit	Note
Supply Voltage	IPS009BL	V_{DD}	-40～85℃	1.2	1.8	3.63	V	V_{DD}
			-40～125℃	1.3	1.8	3.63	V	V_{DD}
	IPS009CM		-40～125℃	1.62		3.63	V	V_{DD}
“H” Input Voltage		V_{IH}		V_{DD}×0.8			V	CE
“L” Input Voltage		V_{IL}				V_{DD}×0.2	V	CE
Input Voltage		V_{IN}		V_{SS}		V_{DD}	V	CE
Output Load Capacitance		CL	CMOS			15	pF	OUT
Ambient Temperature		Topt		-40		125	℃	

This IC has enough immunity against ESD and Latch-up, but handle with care.

5. Electrical Specification

5-1 IPS009BL

Unless otherwise stated, V_{DD}＝1.2V～3.63V, V_{SS}＝0V, T a ＝-40～125℃, f_{xtal}=14～48MHz

Parameter	Symbol	Condition	Specification				Unit
			Min	Typ	Max	125℃	
Out put Leak current	Iz	CE≦0.3V, X1=VDD, Vss, Vout=Vss～VDD			10	15	μA
“H” input current	I_{IH}	CE pad, VIN=VDD	0		0.03	←	μA
“L” input current	I_{IL}	CE pad, VIN=VSS	-0.08		-0.01	←	μA
Oscillation Disable Time	Tplz	OUT pad			0.1	←	μs
Oscillation Enable Time	Tpzl	OUT pad			2	←	ms
Oscillation start up time	Tstart	f_{xtal}=27MHz, V_{DD}≧1.2V			2	←	ms
“H” output voltage	V_{OH}	OUT pad, I_{OH}＝-1.0mA	0.9V_{DD}			←	V
“L” output voltage	V_{OL}	OUT pad, I_{OL}=1.0mA			0.1V_{DD}	←	V
Current consumption	I_{DD}	CL=0pF, VDD=1.8V, CE≧VDD-0.3V, F0=27MHz		0.5	0.8	←	mA
		CL=15pF, VDD=1.8V, CE≧VDD-0.3V, F0=27MHz		1.2	1.5	←	
Current consumption at oscillation disable	I_{DDD}	CL=15pF, VDD=3.3V, CE≦0.3V		1.0	1.2	5.0	μA
Frequency V_{DD} deviation	Fvst	V_{DD}=3.0±10%			±1	←	ppm
		V_{DD}=1.8±10%			±2	←	
Output Duty Ratio	Duty	CL=15pF, V_{DD}=1.2～1.62V	40		60	←	%
		CL=15pF, V_{DD}=1.62～3.63V	45		55	←	
Rise time	Tr	CL=15pF, 10～90%V_{DD}, V_{DD}=2.52～3.63V			3.0	4.0	ns
		CL=15pF, 10～90%V_{DD}, V_{DD}=1.2～2.52V			5.0	6.5	
Fall time	Tf	CL=15pF, 10～90%V_{DD}, V_{DD}=2.52～3.63V			3.0	4.0	ns
		CL=15pF, 10～90%V_{DD}, V_{DD}=1.2～2.52V			5.0	6.5	

5-2 IPS009CM

Unless otherwise stated, V_{DD}=1.62V～3.63V, V_{SS}=0V, T a =-40～125℃, f_{xtal}=48～100MHz

Parameter	Symbol	Condition	Specification				Unit
			Min	Typ	Max	125℃	
Out put Leak current	Iz	CE≦0.3V, X1=VDD, Vss, Vout=Vss～VDD			10	15	μA
“H” input current	I_{IH}	CE pad, VIN=VDD	0		0.03	←	μA
“L” input current	I_{IL}	CE pad, VIN=VSS	-1.0		-0.01	←	μA
Oscillation Disable Time	Tplz	OUT pad			0.1	←	μs
Oscillation Enable Time	Tpzl	OUT pad			2	←	ms
Oscillation start up time	Tstart	f_{xtal}=27MHz, V_{DD}≧1.62V			2	←	ms
“H” output voltage	V_{OH}	OUT pad, I_{OH}=-1.0mA	0.9V_{DD}			←	V
“L” output voltage	V_{OL}	OUT pad, I_{OL}=1.0mA			0.1V_{DD}	←	V
Current consumption	I_{DD}	CL=0pF, VDD=1.8V, CE≧VDD-0.3V, F0=77MHz		2.0	3.0	←	mA
		CL=15pF, VDD=1.8V, CE≧VDD-0.3V, F0=77MHz			5.0	←	
Current consumption at oscillation disable	I_{DDD}	CL=15pF, VDD=3.3V, CE≦0.3V		1.0	1.2	5.0	μA
Frequency V_{DD} deviation	Fvst	V_{DD}=3.0±10%			±1	←	ppm
		V_{DD}=1.8±10%			±2	←	
Output Duty Ratio	Duty	CL=15pF, V_{DD}=1.62～3.63V	45		55	←	%
Rise time	Tr	CL=15pF, 10～90%V_{DD}, V_{DD}=2.52～3.63V			3.0	4.0	ns
		CL=15pF, 10～90%V_{DD}, V_{DD}=1.62～2.52V			5.0	6.5	
Fall time	Tf	CL=15pF, 10～90%V_{DD}, V_{DD}=2.52～3.63V			3.0	4.0	ns
		CL=15pF, 10～90%V_{DD}, V_{DD}=1.62～2.52V			5.0	6.5	

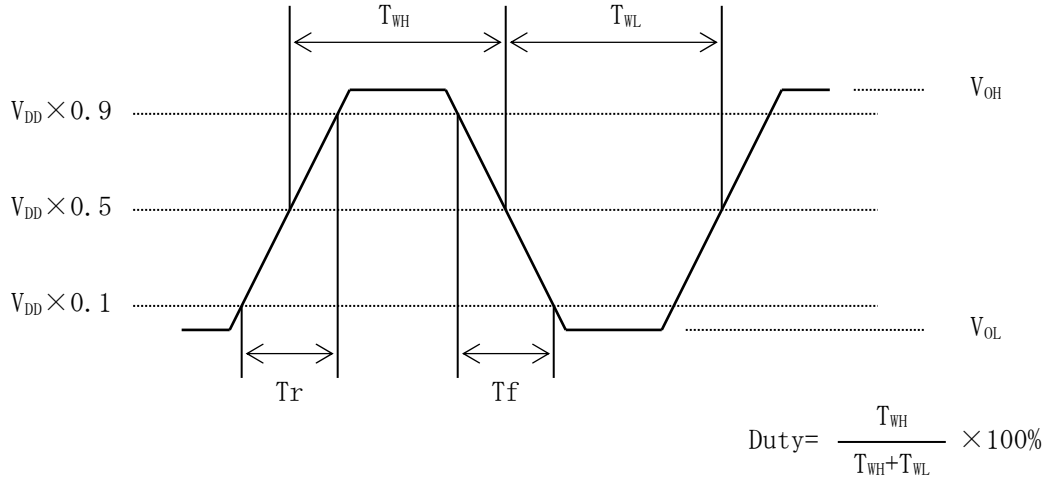
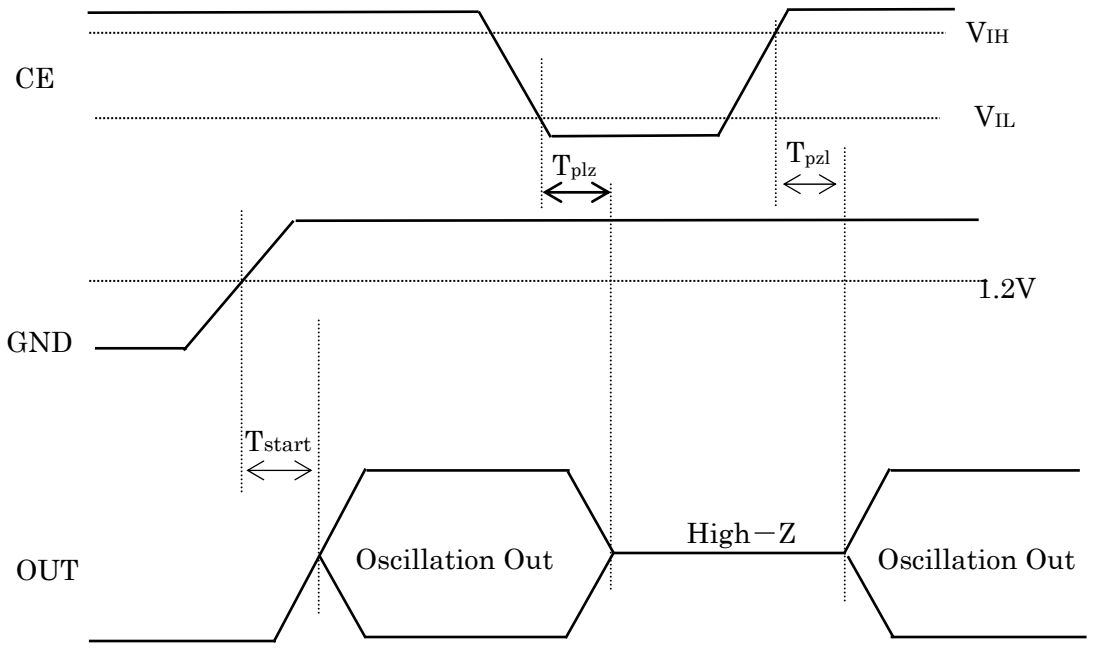


Fig. 5-1 Output wave form (Duty, Tr, Tf, V_{OH}, V_{OL})



V_{IH} : Threshold voltage for Oscillation Start
V_{IL} : Threshold voltage for Oscillation Stop

Fig. 5-2 Input output signal timing

6. Circuit Parameters of Oscillator (Reference Data for Circuit Design)

6-1 IPS009BL Ta =25℃

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Equivalent series (Loading) Capacitance	CLxtal	V_{DD}=2.7V, f_{xtal}=27MHz		4.5		pF
Drive Level	DL	V_{DD}=3.3V, Ta=25℃ f_{xtal}=27MHz		20		μW

*The above values are the design values and are not guaranteed by test.

6-2 IPS009CM Ta =25℃

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Equivalent series (Loading) Capacitance	CLxtal	V_{DD}=2.7V, f_{xtal}=100MHz		7.3		pF
Drive Level	DL	V_{DD}=3.3V, Ta=25℃ f_{xtal}=70MHz		150		μW

*The above values are the design values and are not guaranteed by test.

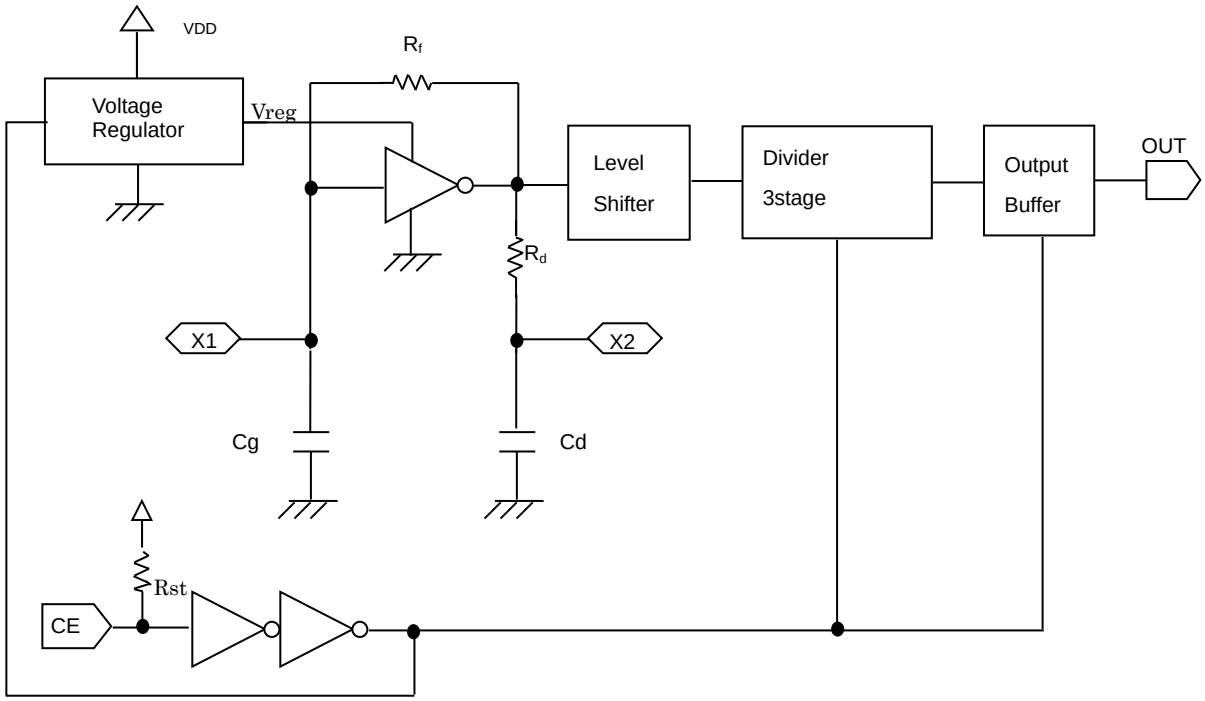
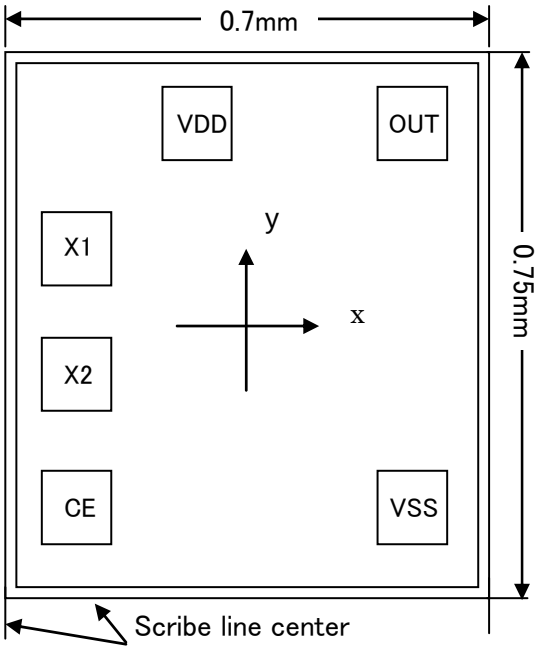


Fig. 6-1 Block Diagram

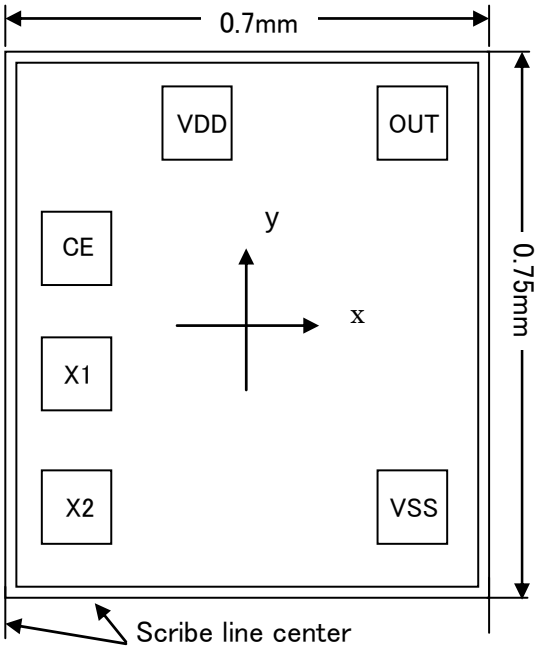
7. Pad Layout



- Die Size : 0.70mm × 0.75mm
- Pad Size : 80um □
- Thickness : 150±20um
- IC Backside : Gnd or Open

Pad Name	Function	Location (μm)	
		x	y
VDD	(+)Power Supply	−105	244
OUT(Q)	Frequency Output	153	244
VSS	(−)Ground	209	−244
CE	Oscillation stop, "L": High-Impedance	−209	−244
X2	Crystal Drive	−209	−74
X1	Crystal Feedback	−209	94
Chip Center		0	0

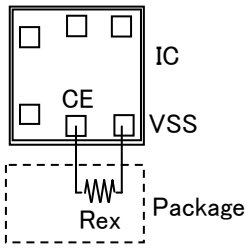
Fig. 7-1 Pad Layout of IPS009BLx-C1 and IPS009CMx-C1 (Straight Type)



- Die Size : 0.70mm × 0.75mm
- Pad Size : 80um □
- Thickness : 150±20um
- IC Backside : Gnd or Open

Pad Name	Function	Location (μm)	
		x	y
VDD	(+)Power Supply	−105	244
OUT(Q)	Frequency Output	153	244
VSS	(−)Ground	209	−244
X2	Crystal Drive	−209	−244
X1	Crystal Feedback	−209	−74
CE	Oscillation stop, "L": High-Impedance	−209	94
Chip Center		0	0

Fig. 7-2 Pad Layout of IPS009BL0-C2 (Cross Type)



IMPORTANT Notice for CE function

* Rex should be over 10MΩ in case of CE = Open usage.
* Oscillation will not be activated when CE = Open after CE = Low if Rex is below 10MΩ.
* There is no such issue in case of CE = VDD usage.

Rex : External resistance value between CE and VSS of package.

■ Description

IPS009BM is the specific SPXO IC for achieving low Phase Noise, corresponding to the fundamental crystal from 14MHZ to 60MHz.

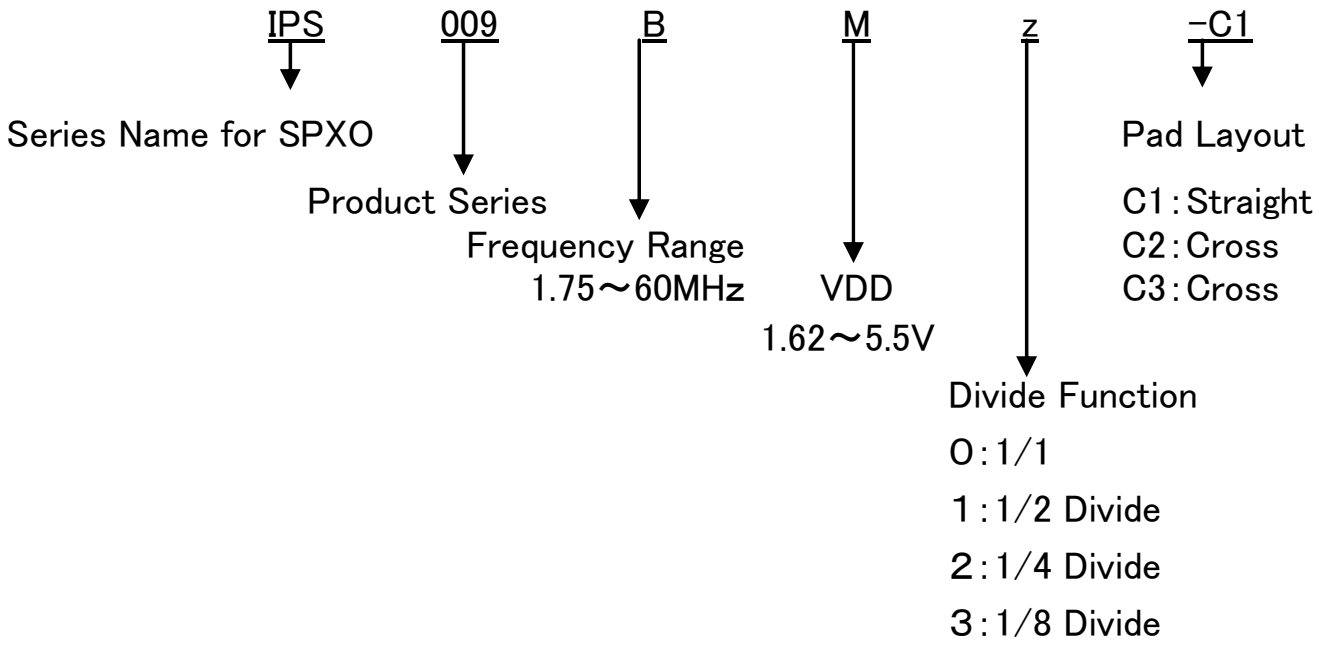
Both the operation temperature (-40℃~125℃) and Vdd range(1.62V~5.5V) is wide, so IPS009BM makes the selection of application wider. If slightly poor phase noise performance is allowed, even 1.8V is applicable.

■ Features

- Phase Noise : -162dBc／Floor 27MHz
- Phase Jitter : 150fsec／27MHz
- Operation temperature : -40℃~125℃
- Power supply voltage : 1.62*1)～2.25～5.5V
- Standby function : Oscillation stop
- Crystal frequency : 60MHz maximum
- Output : CMOS
- Divide function : 1/2, 1/4 and 1/8
- Small chip size : 0.70mm × 0.75mm
- Frequency stability to Vdd : Within ±1ppm
- Duty cycle : Within 50±5%

*1) Phase noise performance becomes slightly poor below 2.25V operation.

1. Part number rule



2. Series

Part Number	Output Frequency (MHz) Min.	Output Frequency (MHz) Max.	Divide	Pad Layout	Vdd (V)	Remarks
IPS009 B M 0 -C1	14.00	60.00	1/1	Straight	1.62 ～ 5.5	Low Phase Noise Wide Vdd
IPS009 B M 1 -C1	7.00	30.00	1/2			
IPS009 B M 2 -C1	3.50	15.00	1/4			
IPS009 B M 3 -C1	1.75	7.50	1/8			
IPS009 B M 0 -C2	14.00	60.00	1/1	Cross		
IPS009 B M 1 -C2	7.00	30.00	1/2			
IPS009 B M 2 -C2	3.50	15.00	1/4			
IPS009 B M 3 -C2	1.75	7.50	1/8			
IPS009 B M 0 -C3	14.00	60.00	1/1			
IPS009 B M 1 -C3	7.00	30.00	1/2			
IPS009 B M 2 -C3	3.50	15.00	1/4			
IPS009 B M 3 -C3	1.75	7.50	1/8			

3. Absolute Maximum Ratings Vss=0V, Ta=25℃±2℃

Parameter	Symbol	Condition	Ratings Min	Ratings Max	Ratings Unit
Supply Voltage	V_{DD}		V_{SS}-0.5	7.0	V
Input Voltage	V_{IN}	All Input Pin	V_{SS}-0.5	V_{DD}+0.5	V
Output Voltage	V_{OUT}		V_{SS}-0.5	V_{DD}+0.5	V
Input Current	I_{IN}	CE Pin		50	μA
Output Current	I_{OUT}			25	mA
Junction Temperature	Tj		-55	150	℃
Storage Temperature	Tstg		-55	125	℃

4. Recommended Operating Condition V_{SS}=0V, T a =- 40℃～＋125℃

Parameter		Symbol	Condition	Min	Typ	Max	Unit	Note
Supply Voltage	IPS009BM		-40～125℃	1.62*1)	3.3	5.5	V	V_{DD}
"H" Input Voltage		V_{IH}		V_{DD}×0.8			V	CE
"L" Input Voltage		V_{IL}				V_{DD}×0.2	V	CE
Input Voltage		V_{IN}		V_{SS}		V_{DD}	V	CE
Output Load Capacitance		CL	CMOS			15	pF	OUT
Ambient Temperature		Topt		-40		125	℃	

*1) Phase noise performance becomes slightly poor at 1.62～2.25V.

This IC has enough immunity against ESD and Latch-up, but handle with care.

5. Electrical Specification

Unless otherwise stated, V_{DD}=1.62V～5.5V, V_{SS}=0V, T a =-40～125℃, f_{xtal}=14～60MHz

Parameter		Symbol	Condition	Specification				Unit
				Min	Typ	Max	125℃	
Out put Leak current		Iz	CE=0V, X1=V_{DD}, Vss, Vout=Vss～V_{DD}			10	15	μA
"H" input current		I_{IH}	CE pad, V_{IN}=V_{DD}	0		0.1	←	μA
"L" input current		I_{IL}	CE pad, V_{IN}=V_{SS}	-1		-0.01	←	μA
Oscillation Disable Time		Tpd	OUT pad			0.1	←	μs
Oscillation Enable Time		Tpe	OUT pad			2	←	ms
Oscillation start up time		Tstart	f_{xtal}=27MHz, VDD≧1.62V			2	←	ms
"H" output voltage		V_{OH}	OUT pad, I_{OH}=-1.0mA	0.9V_{DD}			←	V
"L" output voltage		V_{OL}	OUT pad, I_{OL}=1.0mA			0.1V_{DD}	←	V
Current consumption		I_{DD}	CL=15pF, VDD=1.8V, CE≧VDD-0.3V, F0=27MHz		1.5	2.3	←	mA
			CL=15pF, VDD=3.3V, CE≧VDD-0.3V, F0=27MHz		2.8	4.2	←	
Current consumption at oscillation disable		I_{DDD}	CL=15pF, VDD=3.3V, CE≦0.3V		1.0	1.2	5.0	μA
Frequency V_{DD} deviation		Fvst	V_{DD}=5±10%			±1	←	ppm
			V_{DD}=3.3±10%			±1	←	
			V_{DD}=2.5±10%			±1	←	
Duty Ratio	Except below	Duty	CL=15pF	45		55	←	%
	IPS009BM0-C3		CL=15pF, VDD=1.8±10%	40		60	←	
Rise/Fall time		Tr/Tf	CL=15pF, 10～90%VDD, VDD=1.62～2.52V			5.0	6.5	ns
Rise/Fall time		Tr/Tf	CL=15pF, 10～90%VDD, VDD=2.52～5.5V			3.0	4.0	ns

Phase Noise : Frequency =27MHz, V_{DD} = 3.3V

Offset	IPS009BMx-C1/C2	IPS009BMx-C3
	Phase Noise (dBc)	
1Hz	-75	-76
10Hz	-106	-106
100Hz	-132	-133
1KHZ	-145	-146
10KHz	-154	-157
100KHz	-160	-163
1MHz	-162	-165
Phase Jitter	143fsec	102fsec

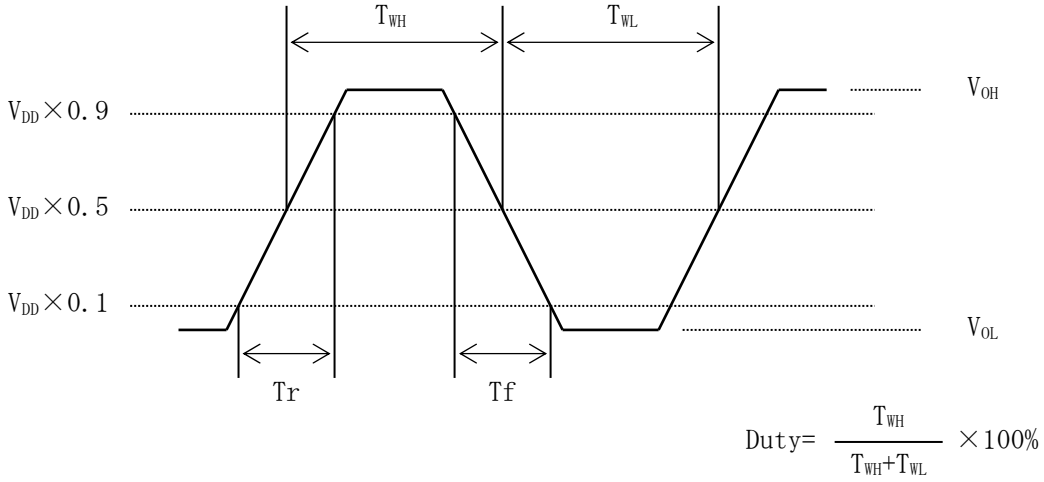
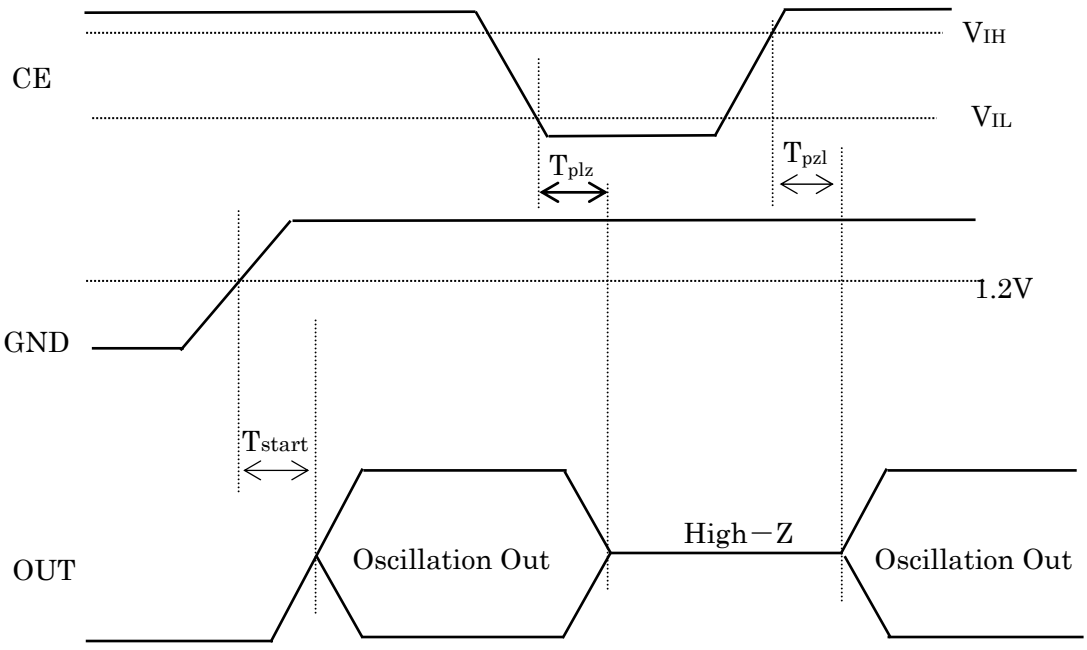


Fig. 5-1 Output wave form (Duty, Tr, Tf, V_{OH}, V_{OL})



V_{IH} : Threshold voltage for Oscillation Start
V_{IL} : Threshold voltage for Oscillation Stop

Fig. 5-2 Input output signal timing

6. Circuit Parameters of Oscillator (Reference Data for Circuit Design) Ta =25℃

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Equivalent series (Loading) Capacitance	CLxtal	V_{DD}=2.7V, f_{xtal}=27MHz		6		pF
Drive Level	DL	V_{DD}=3.3V, Ta=25℃ f_{xtal}=27MHz		60		μW

*The above values are the design values and are not guaranteed by test.

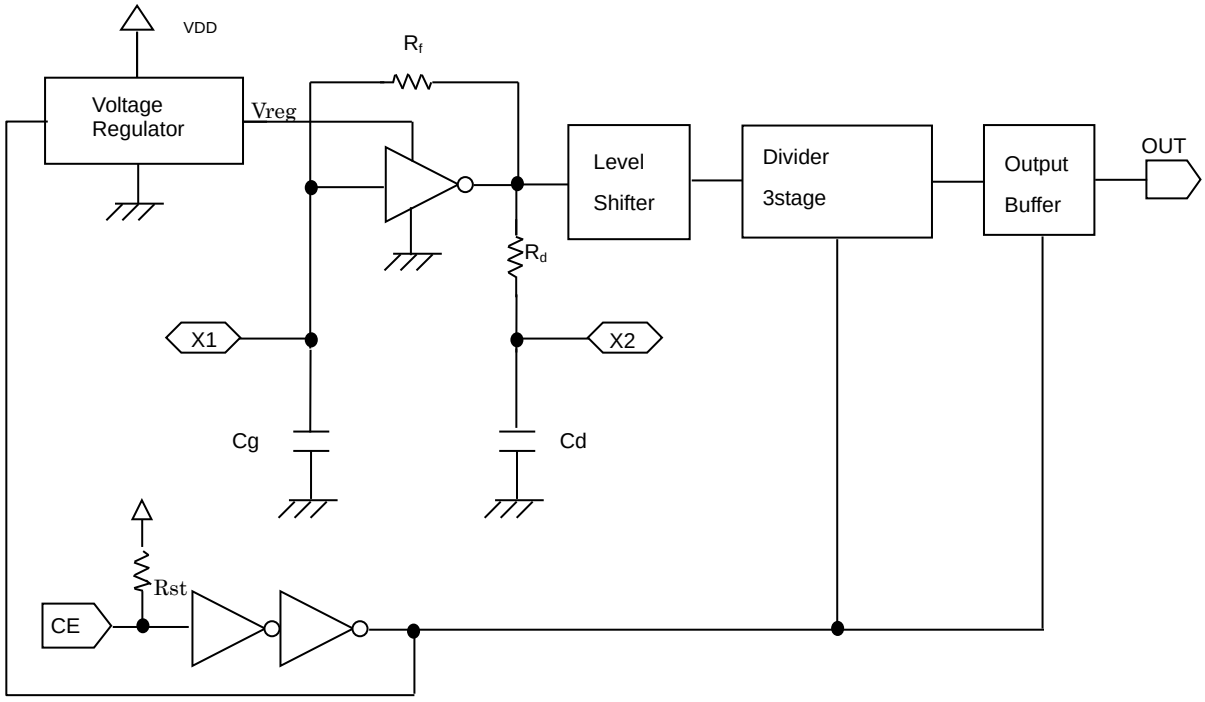
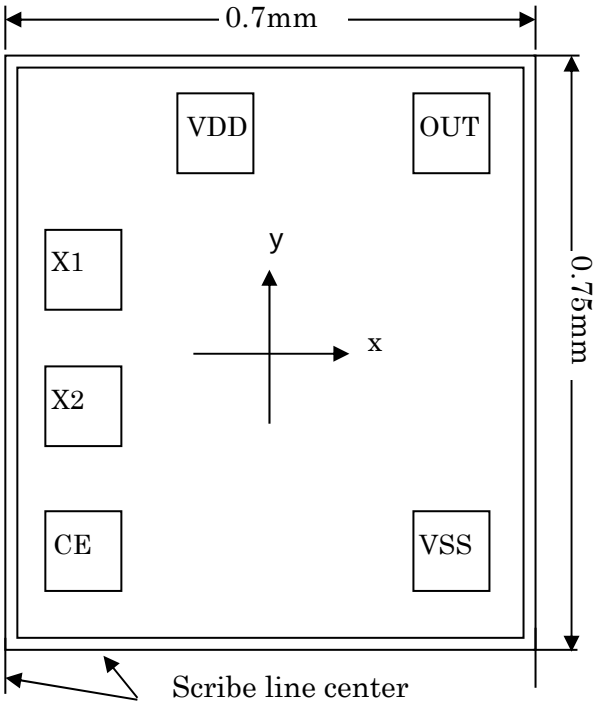


Fig. 6 Block Diagram

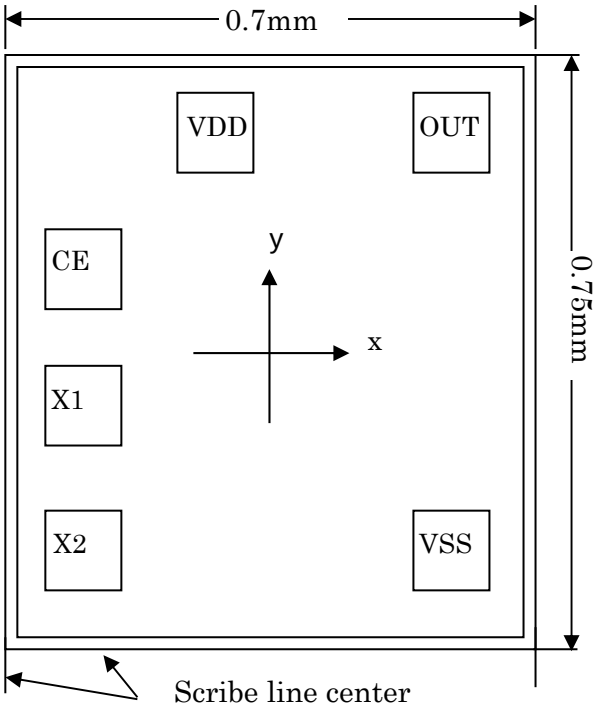
7. Pad Layout



- Die Size : 0.70mm × 0.75mm
- Pad Size : 80um □
- Thickness : 150±20um
- IC Backside : Gnd or Open

Pad Name	Function	Location (μm)	
		x	y
VDD	(+)Power Supply	−105	244
OUT(Q)	Frequency Output	153	244
VSS	(−)Ground	209	−244
CE	Oscillation stop, "L": High-Impedance	−209	−244
X2	Crystal Drive	−209	−74
X1	Crystal Feedback	−209	94
Chip Center		0	0

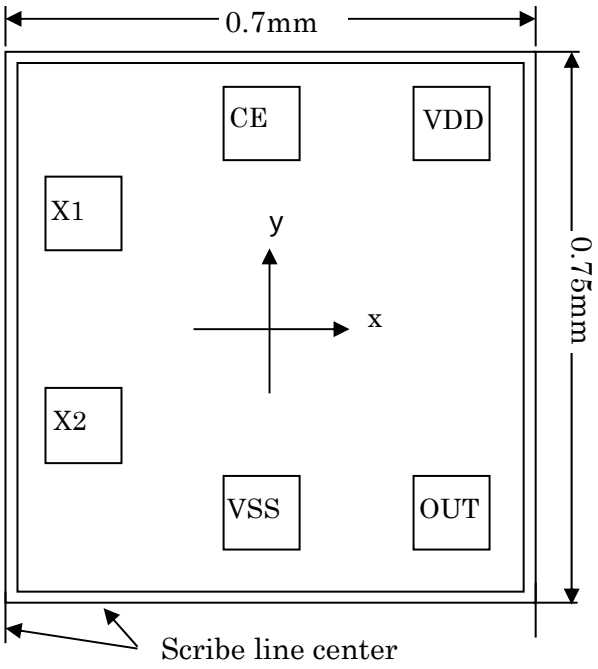
Fig. 7-1 Pad Layout of IPS009BM-C1 (Straight Type)



- Die Size : 0.70mm × 0.75mm
- Pad Size : 80um □
- Thickness : 150±20um
- IC Backside : Gnd or Open

Pad Name	Function	Location (μm)	
		x	y
VDD	(+)Power Supply	−105	244
OUT(Q)	Frequency Output	153	244
VSS	(−)Ground	209	−244
X2	Crystal Drive	−209	−244
X1	Crystal Feedback	−209	−74
CE	Oscillation stop, "L": High-Impedance	−209	94
Chip Center		0	0

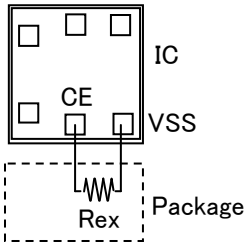
Fig. 7-2 Pad Layout of IPS009BM-C2 (Cross Type)



- Die Size : 0.70mm × 0.75mm
- Pad Size : 80um □
- Thickness : 150±20um
- IC Backside : Gnd or Open

Pad Name	Function	Location (μm)	
		x	y
VDD	(+)Power Supply	152	244
OUT(Q)	Frequency Output	152	−244
VSS	(−)Ground	−39	−244
X2	Crystal Drive	−209	−133
X1	Crystal Feedback	−209	133
CE	Oscillation stop, "L": High-Impedance	−39	244
Chip Center		0	0

Fig. 7-3 Pad Layout of IPS009BM-C3 (Cross Type)



IMPORTANT Notice for CE function

* Rex should be over 10MΩ in case of CE = Open usage.
* Oscillation will not be activated when CE = Open after CE = Low if Rex is below 10MΩ.
* There is no such issue in case of CE = VDD usage.
  Rex : External resistance value between CE and VSS of package.